DRP* TECHNOLOGY ENABLES A HYBRID APPROACH FOR EMBEDDED VISION SOLUTIONS

* DYNAMICALLY RECONFIGURABLE PROCESSOR

NOVEMBER 13, 2019
GREG LARA
SENIOR PRODUCT MARKETING MANAGER
COGNITIVE PRODUCTS DEPARTMENT
ENTERPRISE INFRASTRUCTURE BUSINESS DIVISION
RENESAS ELECTRONICS CORPORATION
AGENDA

- Renesas introduction
- The Vision Processing Challenge
- Dynamic Reconfigurable Processor (DRP) Technology Overview
- RZ/A2M MPU with DRP Technology
- DRP Application Solutions
- Design Resources for RZ/A2M MPU with DRP Technology
WHO WE ARE
THE WORLD’S LEADING EMBEDDED SOLUTION PROVIDER

Originating from Hitachi, Mitsubishi, NEC, and Intersil
Net sales 757.4 billion yen in 2018
19,000+ employees worldwide
Headquartered in Tokyo, Japan

2002
NEC Electronics
Spin-off from NEC

2003
Renesas Technology
Spin-off from Hitachi and Mitsubishi merger

2010
Renesas Electronics
started operation
NEC Electronics and Renesas Technology merged

2017
Acquisition of Intersil
Strengthen leadership
in the analog market

2019
Acquisition of IDT
Integrated Device Technology:
the leading supplier of analog
mixed-signal products including
sensors, connectivity and
wireless power
## RENESAS BROAD PRODUCT PORTFOLIO

### Microcontrollers and Microprocessors

<table>
<thead>
<tr>
<th>Product</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>RL7B</td>
<td>8/16-bit Ultra-Low Energy MCU &lt;br&gt;Sensing and Motor Control</td>
</tr>
<tr>
<td>RX</td>
<td>32-bit High Power Efficiency MCU &lt;br&gt;Motor Control</td>
</tr>
<tr>
<td>RA</td>
<td>32-bit Arm® Cortex®-M MCU &lt;br&gt;Advanced Security, Connectivity &amp; Flexible SW</td>
</tr>
<tr>
<td>RZ</td>
<td>32/64-bit Arm®-based High-End MPU &lt;br&gt;Human Machine Interface, AI Inferencing &lt;br&gt;Industrial Network &amp; Real-time Control</td>
</tr>
<tr>
<td>RE</td>
<td>SOTB™ Process-based &lt;br&gt;Energy Harvesting Embedded Controller &lt;br&gt;Battery maintenance-free IoT devices</td>
</tr>
<tr>
<td>RH850</td>
<td>Renesas 40nm process MCU &lt;br&gt;Automotive only &lt;br&gt;Rich functional safety and security features</td>
</tr>
</tbody>
</table>

### Analog & Mixed Signal, Power Discrete

- Analog Products
- Battery Management IC
- Clock & Timing, Digital Logic
- Interface & Connectivity
- Memory
- Optoelectronics
- Power Devices
- RF Products
- Sensor Products
- Space & Harsh Environment
- Video & Display IC
- Wireless Power

...and more

### SoC, Integrated Platforms

<table>
<thead>
<tr>
<th>Platform</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>Automotive</td>
<td></td>
</tr>
<tr>
<td>Factory automation</td>
<td></td>
</tr>
<tr>
<td>Renesas autonomy™</td>
<td>Automotive</td>
</tr>
<tr>
<td>Renesas RZ/G Linux</td>
<td>Industrial, HMI</td>
</tr>
<tr>
<td>Renesas Synergy™</td>
<td>IoT and IIoT</td>
</tr>
</tbody>
</table>
IMAGE PROCESSING MARKET DYNAMICS
VISION EVOLUTION DRIVES NEED FOR MORE COMPUTING POWER AND CONNECTIVITY BANDWIDTH

Resolution

8MP+
5MP
3MP
2MP
1MP
VGA

More Computing Power, More Bandwidth

130x

Security, Marketing
Network Video
Intruder Alarm
Access Control
Marketing Camera

Consumer Healthcare

Digital Microscope
Medical Camera (Endoscope)
Visual Inspection
Barcode, Character
Picking, Sorting
Motion Capture, Sports Analysis

1x
26x
5x

30
60
100
150+

FPS
EMBEDDED VISION PROCESSING DESIGN GOALS

- High performance
  - More pixels
  - Higher frame rates
- Low power consumption
  - Battery powered operation
  - Thermal dissipation
- Small form factor
  - Hand held
  - Sealed enclosures
- Low cost
  - BOM complexity
  - Manufacturing complexity
- Fast time to market
  - Flexible design
EXISTING ARCHITECTURES

- Software + Processor
  - Multi-core
  - Faster clock

- Hard IP
  - Dedicated hardware
  - Optimized circuit

- FPGA
  - Field programmable hardware
  - Pipelined performance
MULTI PROCESSOR PROBLEM: AMDAHL'S LAW
SPEEDUP IS LIMITED BY THE SERIAL PART OF THE PROGRAM

Amdahl’s Law

Parallel portion
- 50%
- 75%
- 90%
- 95%

https://en.wikipedia.org/wiki/Amdahl%27s_law#
MULTI PROCESSOR PROBLEM: VON NEUMANN ARCHITECTURE
DATA TRANSFER DRIVES POWER CONSUMPTION

Conventional Software Implementation (CPU/DSP/GPU)

Sequential functions with many memory accesses
→ Consuming power with each data transfer

Wired Logic Architecture (ASIP/FPGA)

Saving memory access by combining multiple functions
→ Reducing power by minimizing memory access

References:
- Presentation by Bert Moons
- Relative energy consumption per equivalent MAC operation

Reference: presentation by Bert Moons
HARD IP TRADEOFF
FUNCTIONALITY INCREASE AT COST OF LARGER DIE SIZE AND POWER CONSUMPTION
HARD IP LIMITATIONS
LIMITED FLEXIBILITY TO FIX BUGS FOR PRE-PRODUCTION AND MASS PRODUCTION

What if we find the bug in the field?

Functionality, Cost, Power

Product Generation

Gen 1

Gen 2

Gen 2.1

Gen 2.2

Bug Found!

Reduce Features

Re-spin!

Bug Fix

Upgrade

Optimize

after market

Time-to-market
FPGA CHALLENGES
SILICON OVERHEAD, EFFICIENT MAPPING, SCALING

- Programmability requires tradeoff of increased die size, power, and cost
- Mapping design efficiently to FPGA resources is difficult
- Adding new features may force move to larger, more expensive, and power-hungry FPGA
LIMITATIONS OF EXISTING ARCHITECTURES

- Multi processor
  - Limited scalability
  - Power hungry

- Hard IP
  - Adding functionality increases cost and power consumption
  - Not flexible

- FPGA
  - Power hungry
  - Area efficiency challenge
HARDWARE / SOFTWARE TRADEOFF

Flexibility vs. Performance

- **Software CPU**
  - High flexibility
  - Limited performance

- **Hardware FPGA / ASIC**
  - High performance
  - Low flexibility
COMBINE PROCESSOR + FPGA?

Penalty:
- Cost
- Power
- Heat
- Size
- Complexity
Dynamically Reconfigurable Processor Technology

A Renesas Proprietary Accelerator Technology
Software Flexibility with Hardware Performance

- Software CPU
- Hardware FPGA / ASIC
- DRP

Flexibility: Low to High
Performance: Low to High
DYNAMICALLY RECONFIGURABLE PROCESSOR TECHNOLOGY

Award Winning Technology
Recognized Around the World

December 2018
Electronic Products (US)
1st

April 2019
CITE (China)
1st

October 2019
Elettronica (Italy)
2nd

November 2019
Design World (US)
Silver
PIPKELINED PROCESSING
SPATIALLY EXPANDED DATA PATH

FPGA

Computation / Data Manipulation

Pipelining Registers

Pipelined processing

Spatially expand various operations into LUT architecture

High performance but large die area due to expansion

High performance with area efficiency via Dynamic Reconfiguration

Process spatially expanded operations
Dynamically Reconfigurable Processor Technology

- Spatially expanded time-multiplexed data path
- Hardware IP (Intellectual Property) that can dynamically change its configuration
  - Reduce die area
  - Reduce power consumption
  - Deliver high performance
- Dynamic Reconfiguration changes the configuration of the arithmetic circuit in 1 ns
- Dynamic Loading switches applications in 1 ms
DRP HARDWARE ARCHITECTURE
PE (Processor elements), SRAMs, ALUs, STC (state transition controller), and DMAC

- **Flexible** coarse-grained reconfigurable architecture (Binary/8-bit)
- **Tile-based** scalability (48 PEs x 6 Tiles)
- **Embedded** Intelligent direct memory access controller (DMAC)
Algorithm data path divided into multiple “contexts”
- DRP resources configured by context data
- Context loading directed by state transition controller (STC)

The state defines the data-path structure, which can transition to a new configuration within one clock cycle
DRP PROGRAMMING METHODOLOGY
CREATING CUSTOM CONFIGURED HARDWARE ACCELERATOR

Algorithm expressed in C code

Dedicated Tool Flow
- Synthesis: C to HDL
- Mapping: HDL to DRP resources
- Placement and Routing

Binary for dynamically reconfigurable data path

```
for ( i = 0; i < N; i++) {
    for ( j = 0; j < N; j++) {
        f[i][j] = 5*f[i][j] - f[i][j-1] - f[i-1][j]
                   - f[i+1][j] - f[i][j+1];
    }
}
```
DRP IN THE SYSTEM
RECONFIGURABLE ARRAY + FAST DMA

Reconfigurable Processing Elements Array
- Created pipelined hardware to accelerate algorithm
- Run complex algorithms by switching configurations within a nanosecond (up to 64 contexts)
- Programming with C language via high-level Synthesis tool

Fast and Intelligent Data Mover (DMA)
- Fast external memory access via integrated Direct Memory Access (DMA) controller
- C programming with access API
- Dynamic configuration loading in less 1ms from external memory
DYNAMIC RECONFIGURATION MECHANISM
CYCLE-BASED DATA-PATH CONFIGURATION DIRECTED BY STC (STATE TRANSITION CONTROLLER)

Switch between multiple Data-paths with each DRP clock cycle to execute complex algorithms
Dynamic reconfiguration in one DRP clock cycle
- Up to 64 contexts (HW configurations) stored in DRP
- Context switching managed by State Machine Controller

Dynamic loading of new configuration in as little as 1 ms
- Loads from external memory without interrupting execution
- Change to HW with completely different function set
- Time division execution of huge applications
DRP LIBRARIES
CURRENTLY MORE THAN THIRTY FUNCTIONS AVAILABLE AND MORE ON THE WAY

Real Time Camera Image Processing
- Color conversion
- Image filtering
- Geometric transformations
- Image enhancement

Image Recognition
- Feature detection
- Morphological Transformation
- Other (Reed-Solomon error correction)
USING DRP LIBRARIES
SIMILAR TO USING A DRIVER API

- DRP is on-chip hardware accelerator
- Arm and DRP share system memory
- DRP library incorporated into application code like a driver API
- At run time, DRP:
  - Loads library binaries from Flash (or RAM)
  - Reads data from Input Address
  - Writes data to Output Address
  - Issues interrupt service request (ISR) to Arm processor when task is finished

Program code

- DRP_Load [Library Address]
- DRP_Activate
- DRP_Start [Input_Addr, Output_Addr, etc.]
DRP TECHNOLOGY ENABLES REAL TIME IMAGE PROCESSING

Example Algorithm: Harris Corner Detection boosted 20 X!

<table>
<thead>
<tr>
<th>Execution Time</th>
<th>CPU*</th>
<th>DRP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>235.3 ms</td>
<td>11.6 ms</td>
</tr>
</tbody>
</table>

Frame Rate Comparison (fps)

- CPU: 4 fps
- DRP: 86 fps

* Using Open CV library

Image size: 640 x 480 VGA
Image Color: Grayscale 8BPP
CPU: RZ/A2M Cortex-A9 @528 MHz
DRP: max.66 MHz

© 2019 Renesas Electronics Corporation. All rights reserved.
DYNAMIC LOADING IN MILLISECONDS
ACCELERATE SEQUENTIAL ALGORITHMS / PARALLEL PROCESSING ACROSS MULTIPLE DRP SLICES

Noise Reduction  Canny Edge  Hysteresis Judgement  Overlay and Display

Image Processing in CPU via Sequential Code  CPU

MIPI Camera INPUT

Image: 640x480 VGA, Grayscale 8BPP
CPU: RZ/A2M Cortex-A9 @ 528 MHz
DRP: 66MHz (max)
DYNAMIC LOADING IN MILLISECONDS
ACCELERATE SEQUENTIAL ALGORITHMS / PARALLEL PROCESSING ACROSS MULTIPLE DRP SLICES

Noise Reduction  Canny Edge  Hysteresis Judgement  Overlay and Display

MIPI Camera INPUT

DRP Accelerates Multiple Algorithms via Dynamic Loading

Image: 640x480 VGA, Grayscale 8BPP
CPU: RZ/A2M Cortex-A9 @ 528 MHz
DRP: 66MHz (max)
DYNAMIC LOADING IN MILLISECONDS
ACCELERATE SEQUENTIAL ALGORITHMS / PARALLEL PROCESSING ACROSS MULTIPLE DRP SLICES

Image Processing in CPU via Sequential Code

Image Processing in DRP w/ Dynamic Loading

Noise Reduction  Canny Edge  Hysteresis Judgement

Image Pre-Processing Performance Comparison

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>6 fps</td>
</tr>
<tr>
<td>DRP</td>
<td>90 fps</td>
</tr>
</tbody>
</table>

DRP is 14 x Faster than CPU!
<table>
<thead>
<tr>
<th>Method</th>
<th>Median (us)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Canny (DRP: Dynamic Loading)</td>
<td>1638</td>
</tr>
<tr>
<td>Canny (Edge)</td>
<td>4471</td>
</tr>
<tr>
<td>Canny (Hysteresis)</td>
<td>4685</td>
</tr>
</tbody>
</table>
RZ/A2M MPU WITH DRP TECHNOLOGY
RZ/A2M FOR EMBEDDED REAL TIME IMAGE PROCESSING

Embedded DRP Accelerator
- 10 x the speed of existing CPUs for image pre-processing
- Free DRP libraries for application development

High Capacity Built-in RAM (4 MB)
- Eliminate external DRAM in image-based systems
- Simplifies system design, lowers power consumption, reduces BOM cost

Enhanced Functionality for Vision Applications
- Built-in MIPI-CSI interface for widely available low-cost camera modules
- Image distortion correction hardware Image Renderer (IMR) engine

Vision Applications

- Facial Recognition
- Biometrics
- Barcode Scanners
- Communication Robots
- Home Appliances

© 2019 Renesas Electronics Corporation. All rights reserved.
RZ/A2M – POWER OF AN MPU, USABILITY OF AN MCU

Conventional MPU

- Regulator 3.3V
- Regulator 1.2/1.8V
- DDR2 or DDR3
- SPI Flash
- MIPI Bridge

RZ/A2M Solution

- Regulator 3.3V
- Regulator 1.2/1.8V
- SPI Flash
- RZ/A2M 4MB

Benefits:
- Reduced cost
- Less power consumption
- Reduced area size
- Reduced noise
- Faster startup time
- Simpler design
- Easy QA support
- Easily available
- Supply issue solved

Not needed with RZ/A2M
**RZ/A2M MPU**

**FIRST RZ PRODUCT WITH DRP**

- **Large 4MB SRAM**
  - High-speed access, simplified system design, low BOM cost

- **High performance HMI functions**
  - Cortex-A9 528MHz with NEON
  - 2D Graphics accelerator & Sprite Engine
  - MIPI-CSI camera interface
  - JPEG Hardware codec

- **Rich Connectivity**
  - Dual Ethernet
  - USB/SDHI/MMC/NAND
  - 8-bit DDR memory interface

- **High Security**
  - Trusted Secure IP (TSIP)
  - Hardware crypto acceleration
  - Key management and storage
  - Access management

- **Packages**
  - 324pin BGA: 19mm/0.8mm pitch
  - 272pin BGA : 17mm/0.8mm pitch
  - 256pin BGA: 11mm/0.5mm pitch
  - 176pin BGA: 13mm/0.8mm pitch

---

**System**

| 16 × DMAC  |
| Interrupt Controller  |
| PLL/SSCG  |
| On-chip Debug (JTAG/SWD)  |
| Standby (Sleep/Software/Deep/Module)  |

**CPU**

- Arm Cortex®-A9
  - 528 MHz (1320 DMIPS)
  - 1.2 V (Core), 3.3 V (I/O), 1.8 V (I/O)
  - NEON
  - FPU

**Memory**

- SRAM: 4 MB
- L1 Cache: 32 KB
- D Cache: 32 KB
- L2 Cache: 128 KB

**Timers**

- 3 × 32-bit OSTM
- 1 × 32-bit MTU3
- 8 × 16-bit MTU3
- 8 × 32-bit PWM
- 1 × WDT
- 1 × RTC

**Graphics**

- 1 × CMOS Camera I/F
- 1 × MIPI Camera I/F
- 1 × 2D Graphics Engine
- 1 × Sprite Engine
- Distortion Correction
- 1 × LVDS
- 1 × JPEG Codec Engine

**Analog**

- 8 × 12-bit ADC

**Co-Processor**

- Dynamically Reconfigurable Processor (DRP)
- Secure Boot
- Device Unique ID
- Crypto Engine
- JTAG Disable
- TRNG
- GPIO

**Interfaces**

| 4 × I'C  |
| 2 × SCI  |
| 5 × SCIF (UART)  |
| 3 × RSPI  |
| 2 × CAN-FD  |
| 2 × Ethernet MAC (100M: IEEE1588v2)  |
| 1 × IrDA  |
| 1 × SPDIF  |
| 4 × SSI (I'S)  |
| 1 × BSC (Ext. Bus I/F) w/SDRAM (132 MHz)  |
| 1 × HyperFlash/RAM (133 MHz DTR, 8-bit)  |
| 1 × SPI Multi I/O (DTR) (QSPI/HyperFlash)  |
| 1 × NAND (ONFI 1.0, ECC)  |
| 2 × USB 2.0 High Speed (Host/Peripheral/OTG)  |
| 2 × SDHI (UHS-I)/MMC  |
RZ/A2M SOLUTIONS FOR DRP-ACCELERATED IMAGE PROCESSING
OBJECT DETECTION DEMO CONFIGURATION

CMOS sensor (Raspberry Pi Camera V2)

- Input Image size: 480p/960p
- ROM: 900KB, RAM: 1.5MB (total)
- DRP Library:
  - Simple ISP
  - Sobel
  - Binarization
  - Dilate
  - Erode
  - Find Contour

Display output

Captured image

Display decode result

Data Matrix

OBJECT DETECTION DEMO CONFIGURATION

RZ/A2M Development Board

Brew Pod
OBJECT DETECTION EXECUTION

1. Data matrix detection processing
   - DRP-accelerated pre-processing
   - Input image 480x480
     - Simple ISP: De-mosaic / Noise reduction / AE control
     - Sobel: Extract contour
     - Binarization: Data size reduction by binarization
     - Dilate: Emphasize contour
     - Erode: Remove unnecessary contour
     - Find Contour: Object detection
   - Find areas likely to be data matrix

2. Data matrix decode processing
   - Decode cropped areas likely to be data matrix
     - Crop detection areas
     - Z-Xing (decode processing)
     - Decoding results: Display on LCD.

http://renesas.com

© 2019 Renesas Electronics Corporation. All rights reserved.
OBJECT DETECTION SOLUTION DEMO
RZ/A2M OBJECT DETECTION SOLUTION

Extracts 2D Barcodes from complex label via DRP library that detects and labels contours in input images

DRP Processing Example

Input Image → Simple ISP (De-mosaic, noise reduction) → Sobel → Binarization → Dilate → Erode → Find Contours → Cropping → ZXing (Decode)

DRP Advantage

Processing 5x faster than CPU

CPU: 325 ms
DRP: 72 ms

Applications

- Factory inspection
- Home appliances (Coffee maker, robot vacuum, microwave oven, etc.)
- Home camera etc.

Design Data

- Free download available now
2D BARCODE SCANNING

Design Requirements

High-resolution video input
- Easy to scan at a variety of distances
- Adaptable to different environments

Fast scanning and decoding
- Improved user experience
- Hi-speed production lines

Low power dissipation
- Battery powered handheld devices
- Sealed enclosures for industrial environments
- Ruggedized enclosures for field deployment

Applications
DRP ACCELERATED 2D BARCODE PROCESSING FLOW

- Simple ISP: Demosaicing, Noise reduction
- Binarization: Adaptive, Reduces data
- Marker Detection
- Reed Solomon: Decode process

Auto Exposure: Adjusts brightness
AE improves recognition

DRP-accelerated decoding

http://renesas.com

DRP Library

CPU
RZ/A2M 2D BARCODE DECODING SOLUTION DEMO

2D Barcode Demo
SIMPLE ISP SOLUTION
**RZ/A2M SIMPLE ISP**

The Simple ISP is a DRP library which works with each solution example for increased value

1. **Cost Reduction**: Using MIPI and Simple ISP, systems can be realized with low-cost CMOS sensors
2. **Improved Recognition**: Increased robustness by combining the ISP and Cognitive-specific AE control
3. **High-speed Processing**: The DRP library accelerates image processing

**Example Use**

**Support**
- DRP Library
- 2D Barcode Solution
- IRIS Solution

**Target Device**
- RZ/A2M

**Cognitive Applications**
- Bad Lighting
- Detection
- Extraction
- Recognition

**Feedback**

**DRP Library**

**Image Processing**

**Match!**
MOTION DETECTION AND DYNAMIC CONTROL SOLUTION
MOVING OBJECT TRACKING
INTEGRATED VISION AND MOTION PROCESSING

System layered components

Application Program

- MIPI®
- OpenCV
- Dynamics Lib.
- DRP Lib.
- FreeRTOS™

Drivers

- DRP
- Arm® Cortex®-A9
- SCI

RZ/A2M DEVELOPMENT BOARD
SMALL FORM FACTOR

RZ/A2M Eva-Lite (SEMB1451/1452)
MOVING OBJECT TRACKING
INTEGRATED VISION AND MOTION PROCESSING

Software flow

- Vision Processing
  - Image Capturing
  - Image Preparation*4
    - Find Contour
    - Calculation Target

- Motion Control
  - LPF Target
  - PID Current - Target
  - Calculation of IK
  - Servo Control

*4: Image Preparation: Image Conversion + Shading Correction + Subtraction for Motion Detection + Binarization

Robot arm: OpenMANIPULATOR-X (BIOBOTS Co., Ltd.)
All trademarks and registered trademarks are the property of their respective owners.
MOVING OBJECT TRACKING
DRP-ACCELERATED VISION PROCESSING FLOW

**Image Conversion**
- Bayer-to-RGB
- Resize from VGA to 160x120

**Shading Correction**
- Adjust per-pixel gain to correct vignetting

**Motion Detection**
- Calculate difference between frames

**Binarization**
- Reduce data

**Find Contour**

**DRP-accelerated image pre-processing**

**DRP Library**

**CPU**

© 2019 Renesas Electronics Corporation. All rights reserved.
MOVING OBJECT TRACKING DEMO
INTEGRATED VISION AND MOTION PROCESSING
DESIGN RESOURCES FOR RZ/A2M WITH DRP
# RZ/A2M DEVELOPMENT ENVIRONMENT OVERVIEW

<table>
<thead>
<tr>
<th>Development Tools</th>
<th>Software</th>
<th>Evaluation Boards</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrated Development Environment</td>
<td>Abundant Sample code</td>
<td>Evaluation kit for microprocessors</td>
</tr>
<tr>
<td>e² studio</td>
<td>User Application</td>
<td></td>
</tr>
<tr>
<td>Coding</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Debug</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Extended interfaces for the IDE to support smart development</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Smart Utilities</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- Smart Configurator</td>
<td></td>
<td></td>
</tr>
<tr>
<td>- QE (quick and effective tools)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Partner Products</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RZ/A2M Software Package (BSP)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Middleware</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Device Drivers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRP libraries</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Partner Products</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Partner Products</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
RENESAS TOOLS

Work with Smart Utilities and QE to improve customer development efficiency and shorten development period

Smart Configurator

View memory maps, and configure clock pins and various driver settings through a simple GUI!

Smart Manual

Using the viewer, you can inspect the manual and look up keywords and register names. Just by hovering over register and function names with the mouse cursor, the editor displays a pop-up with an explanation of the specification!

QE

QE for Camera and QE for Display are in planning for the RZ/A2. Easily-to-use GUI for configuring camera and display timing, adjusting image quality and more!

Smart Browser

Enables you to look up the latest hardware manuals, technical updates and application notes for your target device. It’s also possible to import projects in order to view sample code, or projects including sample code!
RZ/A2M SOFTWARE PACKAGE

Free RZ/A2M Software Package

RZ/A2M Software Package

RTOS

Free RTOS

TES Guiliani App

Sample Application

Middleware

eGML*1

DRP Library

Device Driver

DRP Driver

Tool

e2 studio, GSE*2 and other tools

👍 Downloadable from the Renesas Website

👍 Based on FreeRTOS v10

IDE

e2 studio (Eclipse)

Compiler

GNU Arm Embedded Toolchain 6-2017-q2-update

GUI Tool

TES Guiliani-Lite

*1 embedded Graphics Multiplatform Library

*2 Guiliani Streaming Editor

Renesas provides various driver samples and applications to reduce development time

Target Applications

2D Barcode, Iris Detection ... and more to come!
DRP LIBRARIES
CURRENTLY MORE THAN THIRTY FUNCTIONS AVAILABLE AND MORE ON THE WAY

Real Time Camera Image Processing
- Color conversion
- Image filtering
- Geometric transformations
- Image enhancement

Image Recognition
- Feature detection
- Morphological Transformation
- Other (Reed-Solomon error correction)
RZ/A2M EVALUATION KIT

- Complete RZ/A2M Evaluation Platform
- Evaluate DRP technology
- MIPI Camera Module (MIPI CSI)
- HyperFlash™ and HyperRAM™ memory
- RGB conversion board for HDMI display
- Two Ethernet communication channels
- Other peripheral functions: SDHI, USB, etc.
- Segger J-Link Lite debugger

Part number: RTK7921053S00000BE
DRP TECHNOLOGY RESOURCES

Visit RZ/A2M MPU Product Page

- **Watch** Videos: RZ/A2 MPU Overview; DRP Technology Overview; DRP Solution Demos
- **Download** Free Development Tools
- **Download** Free RZA2M Software Package
- **Download** Free RZA2M Demo Designs and Application Guides
- **Buy** RZ/A2M Evaluation Kit

[https://www.renesas.com/rza2m](https://www.renesas.com/rza2m)
SUMMARY AND NEXT STEPS

- Embedded Vision Evolution demands more computing power
- Limitations of available architectures: scalability, power consumption, flexibility, and efficiency
- DRP technology addresses these challenges:
  - Massively-parallel custom-configured pipelined hardware data path
  - Virtually expandable silicon via time domain multiplexing (dynamic reconfiguration)
  - DRP-based solutions accelerate image processing, reduce power, and reduce cost
  - Renesas continues investment in DRP technology to enhance additional applications
THANK YOU
Empowering Product Creators to Harness Embedded Vision

The Embedded Vision Alliance (www.Embedded-Vision.com) is a partnership of 90+ leading embedded vision technology and services suppliers, and solutions providers.

Mission: Inspire and empower product creators to incorporate visual intelligence into their products.

The Alliance provides low-cost, high-quality technical educational resources for product developers.

Register for updates at www.Embedded-Vision.com

The Alliance enables vision technology providers to grow their businesses through leads, ecosystem partnerships, and insights.

For membership, email us: membership@Embedded-Vision.com
The only industry event focused on enabling product creators to create “machines that see”

- “Awesome! I was very inspired!”
- “Fantastic. Learned a lot and met great people.”
- “Wonderful speakers and informative exhibits!”

Embedded Vision Summit 2020 highlights:

- **Inspiring keynotes** by leading innovators
- High-quality, practical **technical, business and product talks**
- Exciting **demos** of the latest apps and technologies

Visit [www.EmbeddedVisionSummit.com](http://www.EmbeddedVisionSummit.com) to sign up for updates