embedded VISION SUMMIT

Vision-Based Automotive Driver Assistance: Challenges and Approaches

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Presentation Outline

- Driver Assistance Systems Development Challenges
- Multi-Camera, Multi-Feature DA Project Description
- Multi-Camera, Multi-Feature DA System Implementation
- Project Results

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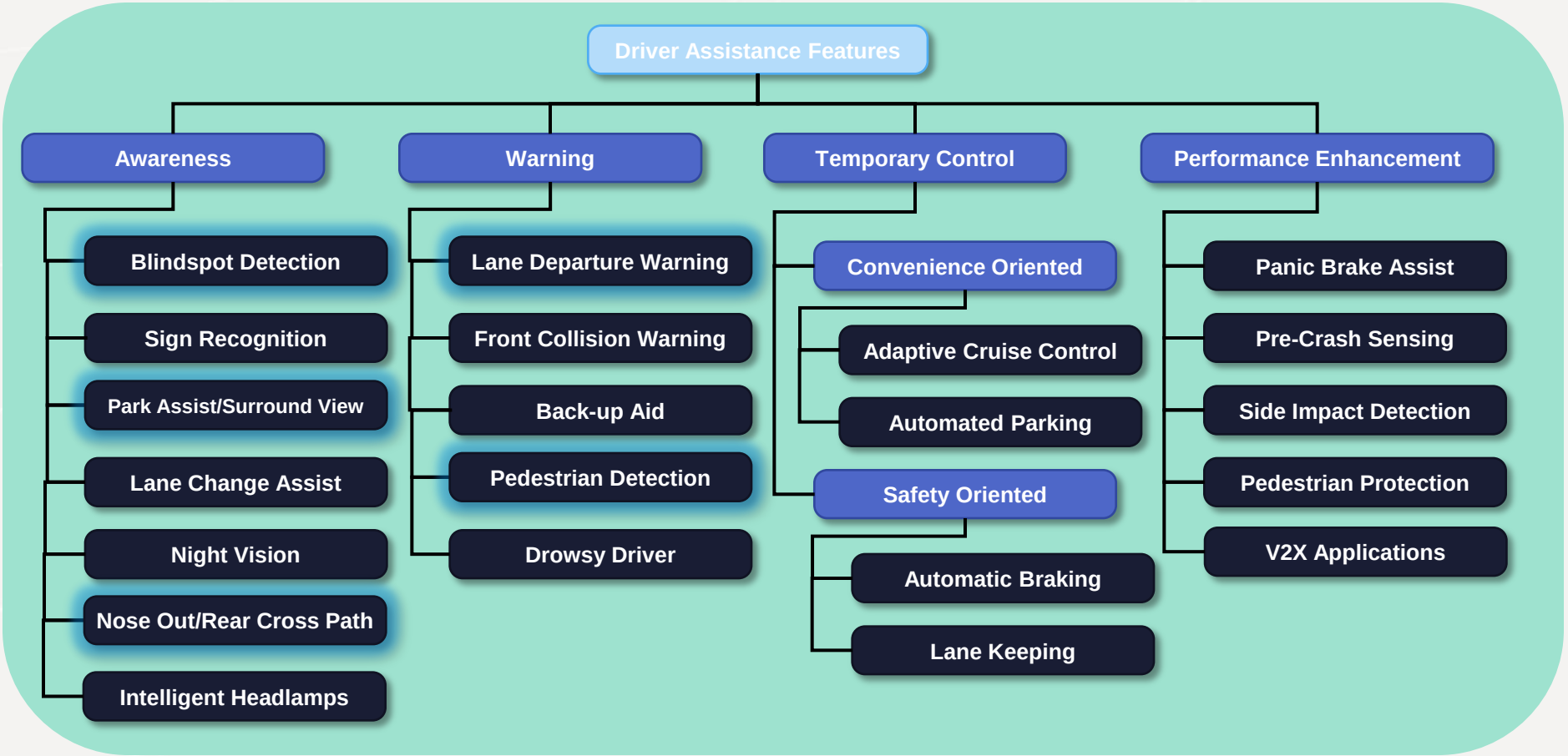
Driver Assistance Systems

Utilizing advanced sensing technologies and processing to *"make drivers better drivers"*



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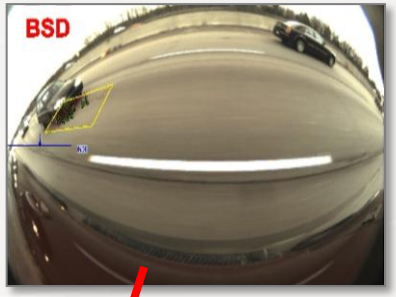
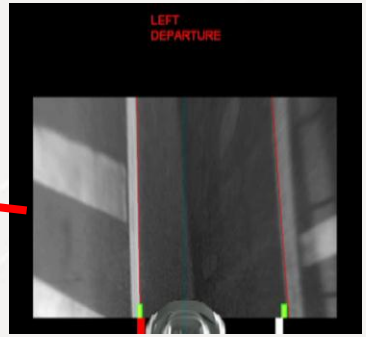
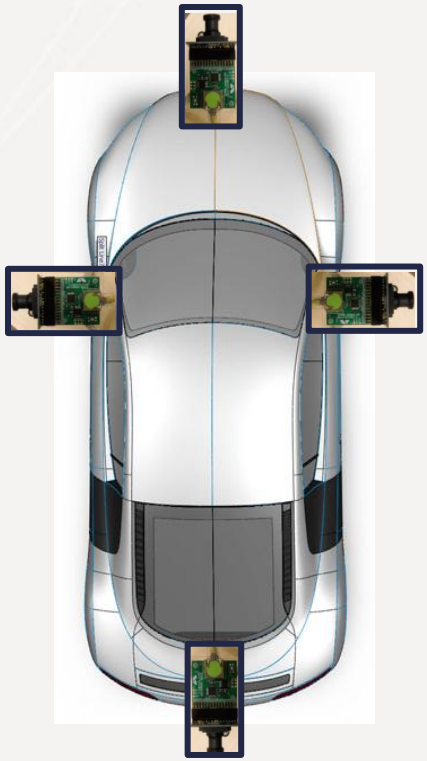
Multi-Feature Bundles / Common Sensor Set







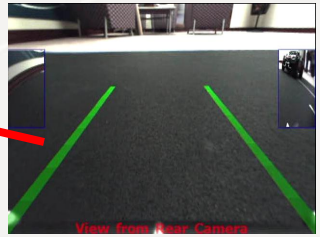
Blindspot Detection

Lane Departure Warning

Park Assist/Surround View

Pedestrian Detection

Nose Out/Rear Cross Path



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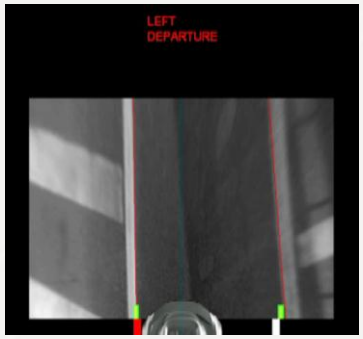

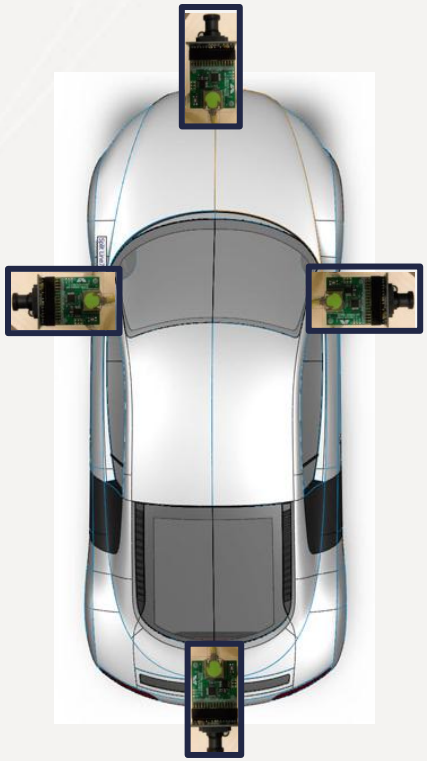

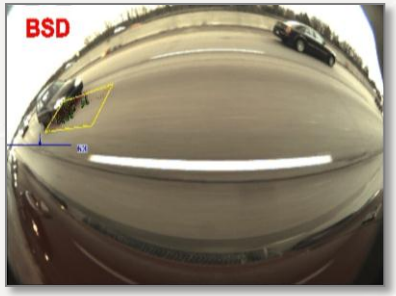

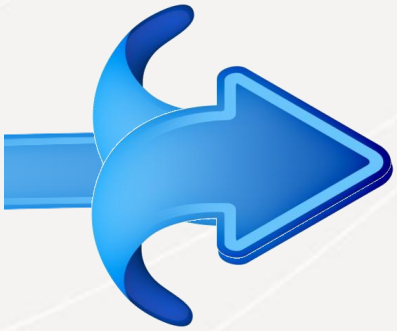

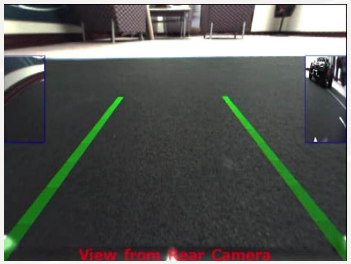

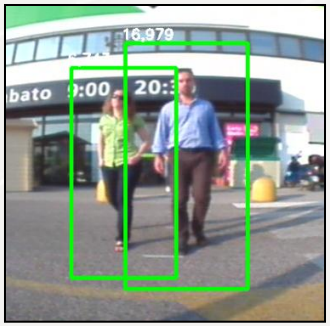

The Platform Challenge:

- **Combining simultaneous multi-feature functionality into a single, efficient processing platform**
- **Maintaining *flexibility* to support alternative feature bundles and *scalability* to meet cost targets for various levels of performance**

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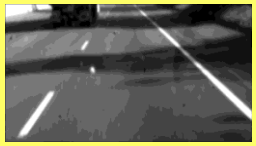
The Partitioning Challenge
Lane Departure Warning Example



Input Image

Pre-Processing (Pixel Level)

- Image Capture, Format Decode
- Progressive Smoothing
- Edge Detection
- Thresholding / Thinning
- Lane Marking Pattern Search

Pre-Processed Image

Analytics Processing (Element Level)

- Road Model Fitting
  - •Data Pt. Table
  - •Model Hypothesis
  - •Pt. Selection
  - •Model Voting
- Lane Tracking (Kalman Filtering)
  - •State Machine Control
  - •Arithmetic Scheduler
  - •Computations

Identified Elements

Application Processing (Frame Level)

- System Finite State Machine
- Vehicle Location wrt to Roadway
- Vehicle Communications (Status and Warning)
- Camera Control

Driver Warning

Computationally Intensive Parallel Processing in Hardware → **Mixture of Serial and Parallel Compatible Functions** → **Serial Decision/Control Processing in CPU**

- **Driver Assistance Processing needs span continuum from computationally intensive functions (parallel process compatible) to decision/control functions (serial process compatible)**
- **Vehicle and sensor connectivity is another critical aspect**

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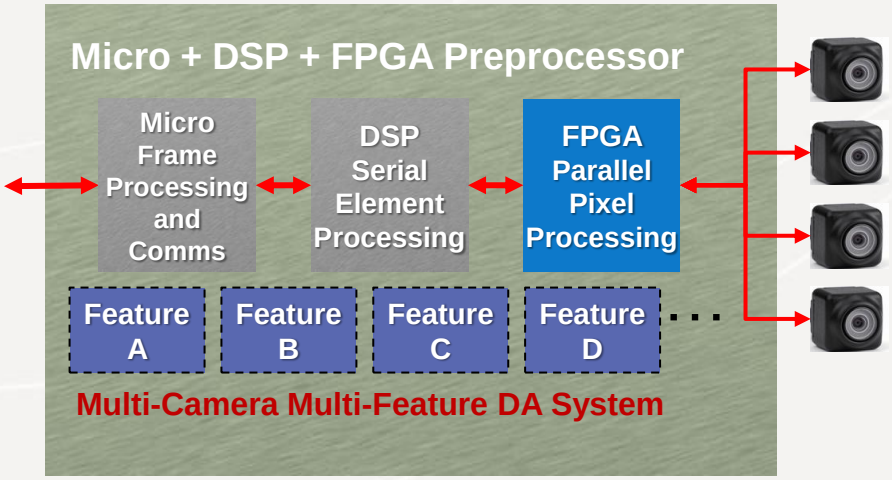
The Architecture Challenges

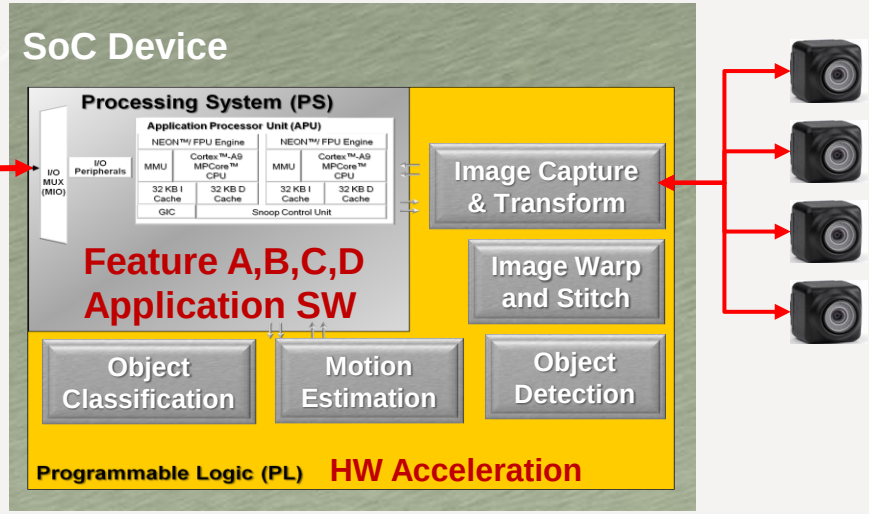
- **Architecture-related Challenges:**
  - Performance for Multiple Features
  - Feature Bundling Variation
  - Algorithmic Flexibility
  - System Power Limitations
  - System Cost Targets

- **Possible/Feasible Approaches:**
  - Parallel Hardware Acceleration
  - Programmable HW as well as SW
  - Bandwidth for flexible HW/SW partitioning
  - Eliminate Chip-to-Chip Interfaces
  - Function integration into a single, scalable device

Traditional Architecture



All Programmable SoC Architecture



Example DA Features

- Blind-spot detection, 360 degree surround view, Lane departure warning, Pedestrian detection

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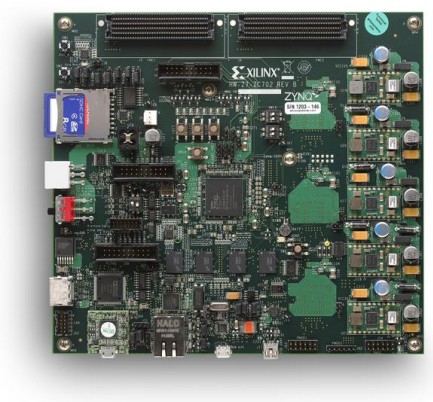
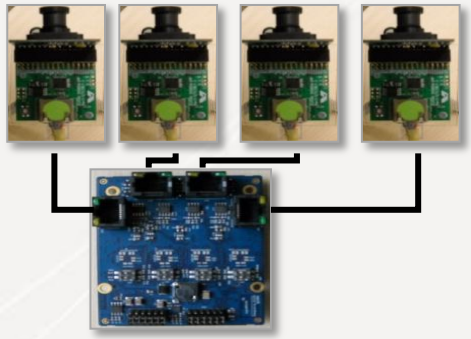
Multi-Camera/Multi-Feature Development Project Low Speed Features—3D Surround View and Pedestrian Detection/Ranging

- ZC702 Development Board

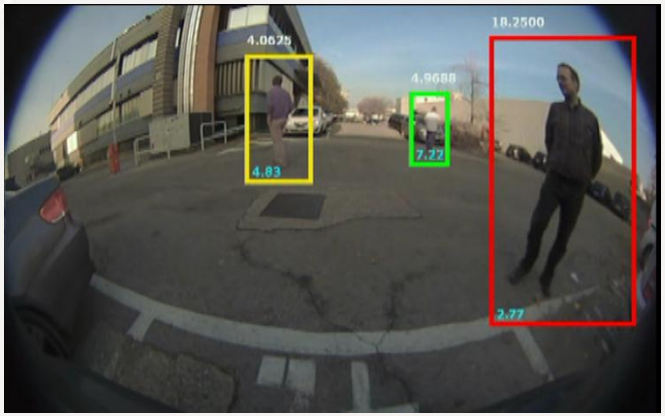


- LVDS Daughter Card & Cameras



- 3D Surround View

- Pedestrian Detection



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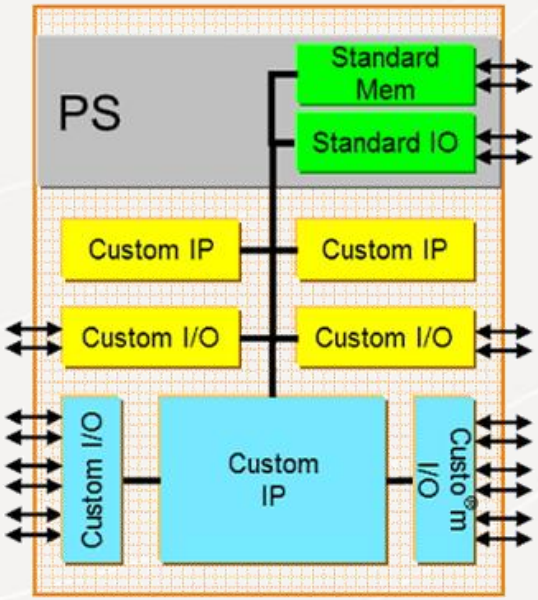
All Programmable SoC Device Processing Models

"All Programmable" refers to ability to not only program an ASSP-like processing system via software methods, but to the programmability (and re-programmability) of hardware accelerators in Programmable Logic (PL) fabric

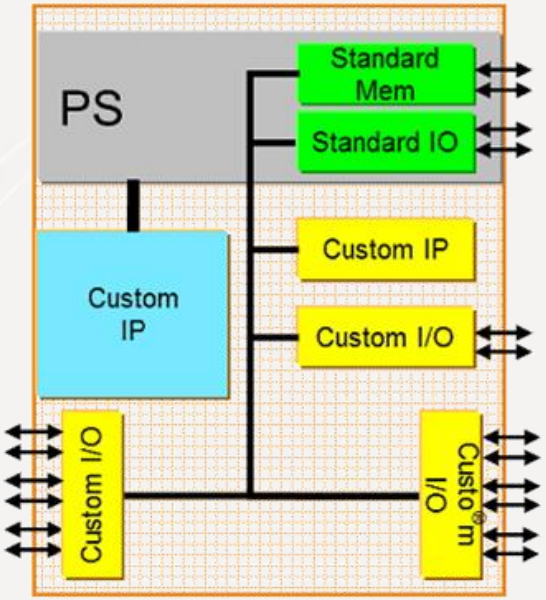
Model 1: Data Flow Model



Control – Data Flow Model

- Custom IP for complex function & data flows
- PS for control & resource management

Model 2: Acceleration Model



Acceleration Model

- Balances SW/HW partition
- PS primary compute platform
- PL for HW Acceleration
- Communication between PS & PL: High

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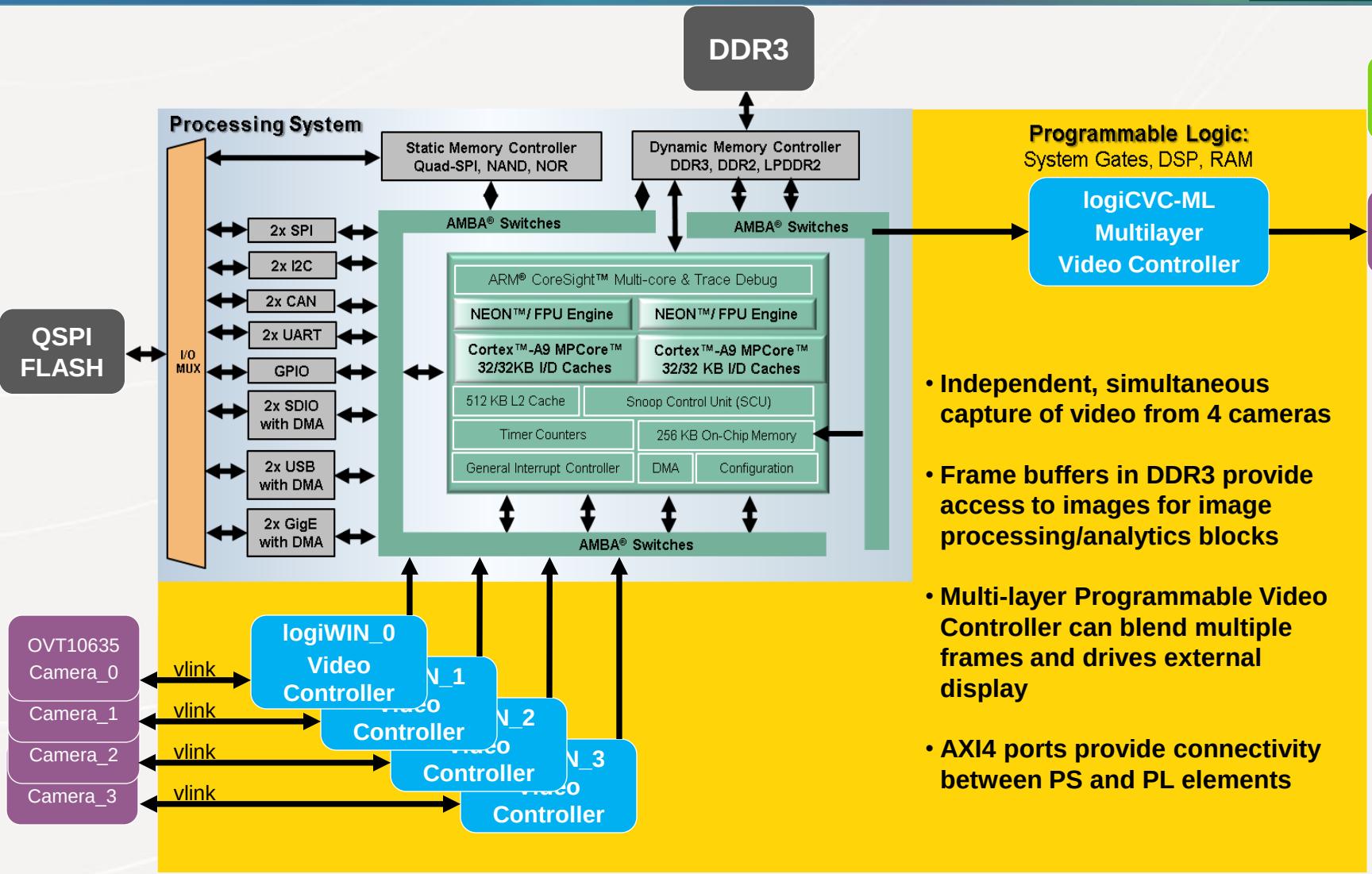
Multi-Feature DA Processing Framework
Video Frame Capture, Frame Buffering, and Display Drive



- **Independent, simultaneous capture of video from 4 cameras**
- **Frame buffers in DDR3 provide access to images for image processing/analytics blocks**
- **Multi-layer Programmable Video Controller can blend multiple frames and drives external display**
- **AXI4 ports provide connectivity between PS and PL elements**

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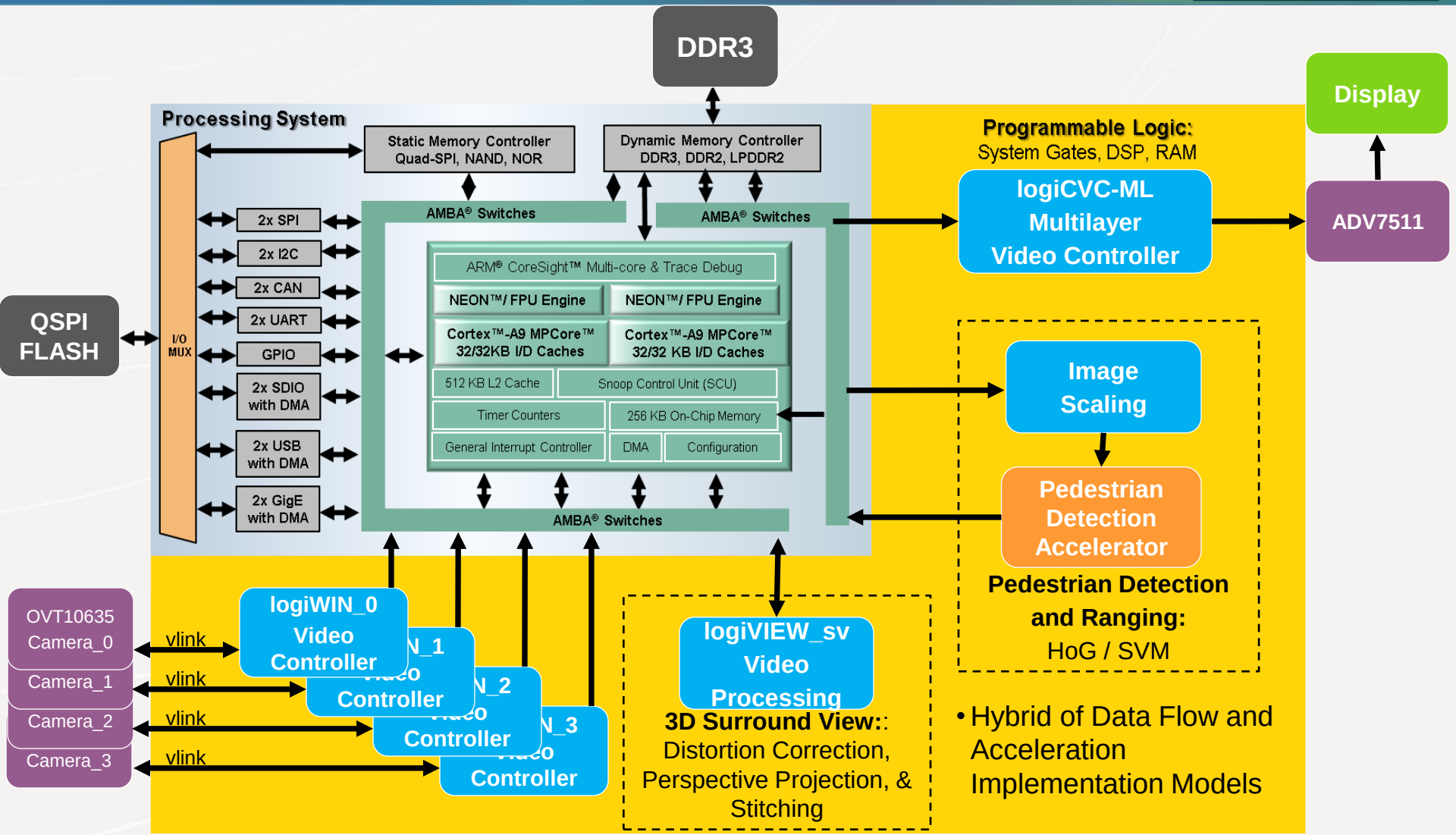
Low Speed Feature Implementation
3D Surround View, Pedestrian Detection (and Ranging)



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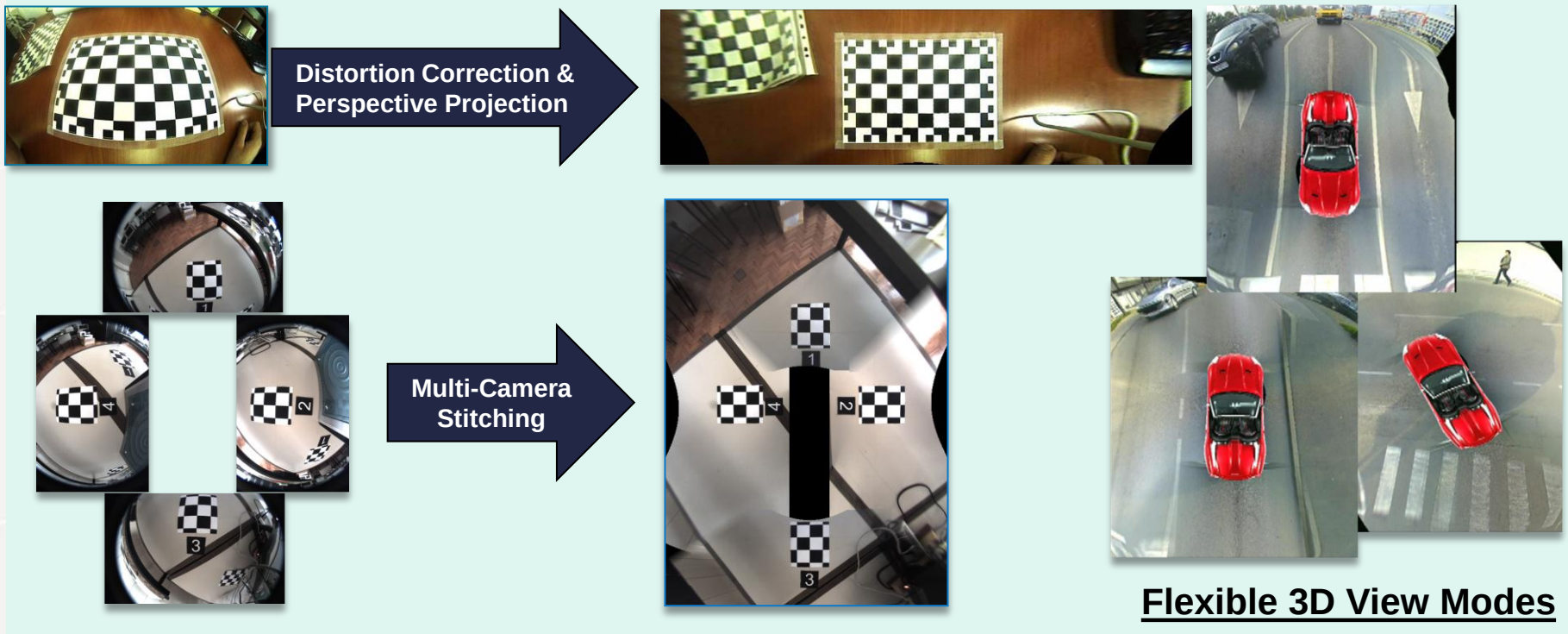
Surround View Processing
Data Flow Implementation Model

- "logiVIEW" provides lens distortion correction, perspective projection and multi-camera stitching functionality



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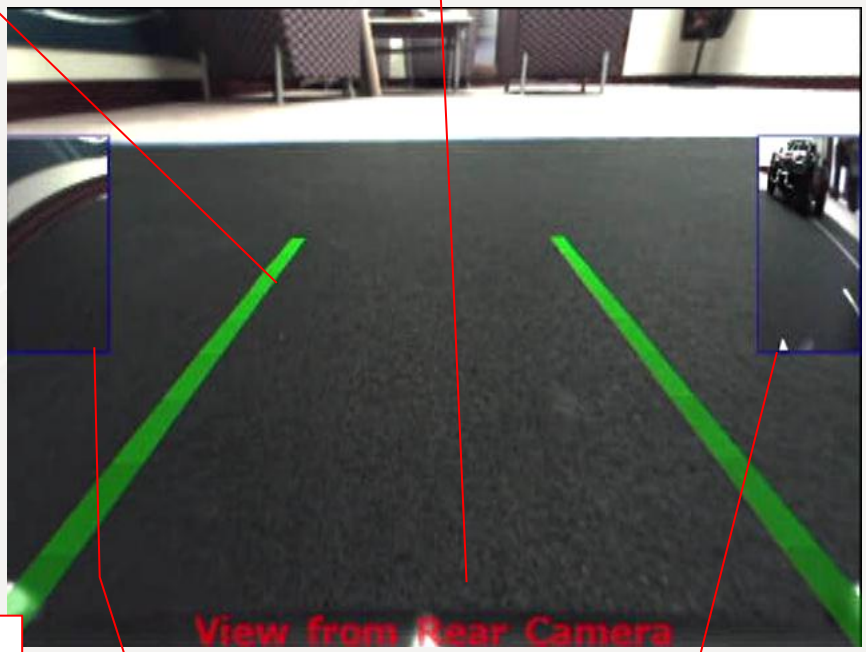
Multiple Video Paths and Display Modes
Surround View, Rear View Camera, and Rear Cross Path

Graphical overlays and text placed on a separate layer with their own CLUT and alpha blending



Hybrid images comprised of different “views of interest”

Overlay/integration of JPEG/BMP/JPEG images

Images from different cameras placed on separate layers and alpha-blended at the seams

Picture-in-Picture (PiP) images for displaying situation dependent views (e.g. rear cross traffic shown)

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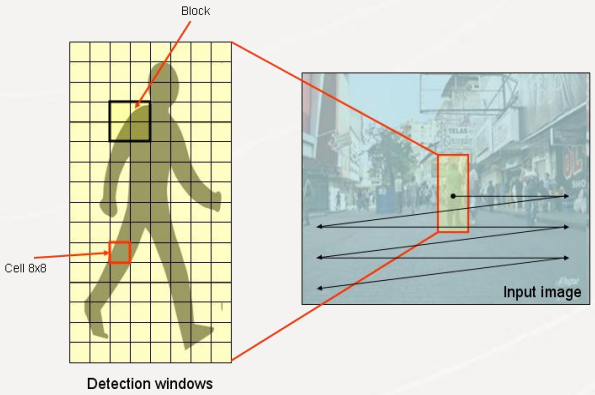
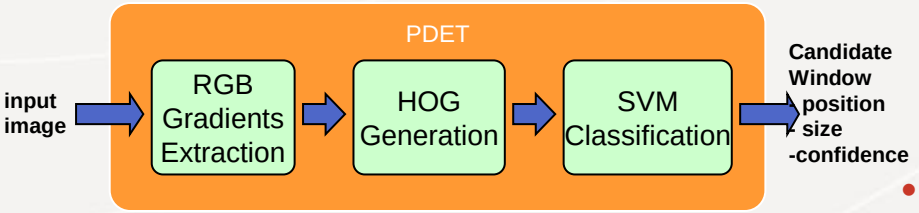
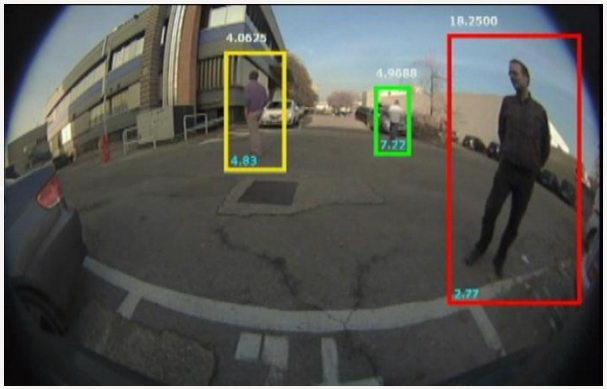
Pedestrian Detection/Classification
HoG/SVM Approach





- Pedestrian Detection



- **Acceleration Block Functionality**
  - Detection Window is scanned across frame
  - The HoG descriptor of the window is evaluated by the SVM to generate a pedestrian detection confidence value for each window location
  - To allow for detection of pedestrians of different sizes and ranges, the core is preceded by an image scaler which generates 17 different scales per frame
- **Acceleration Block Performance (not considering the scaler)**
  - The core utilizes 35 DSP48 blocks. 32 of them operate in parallel at 200 MHz. Consider only those results in 6.4 GMAC/sec (Theoretically these blocks could run at 224 MHz for 7.168 GMAC/sec)
  - Summing all simple operations performed within the algorithm (e.g. add, sub, cmp, atan, div, sqrt) results in @ 30 GOPs/sec

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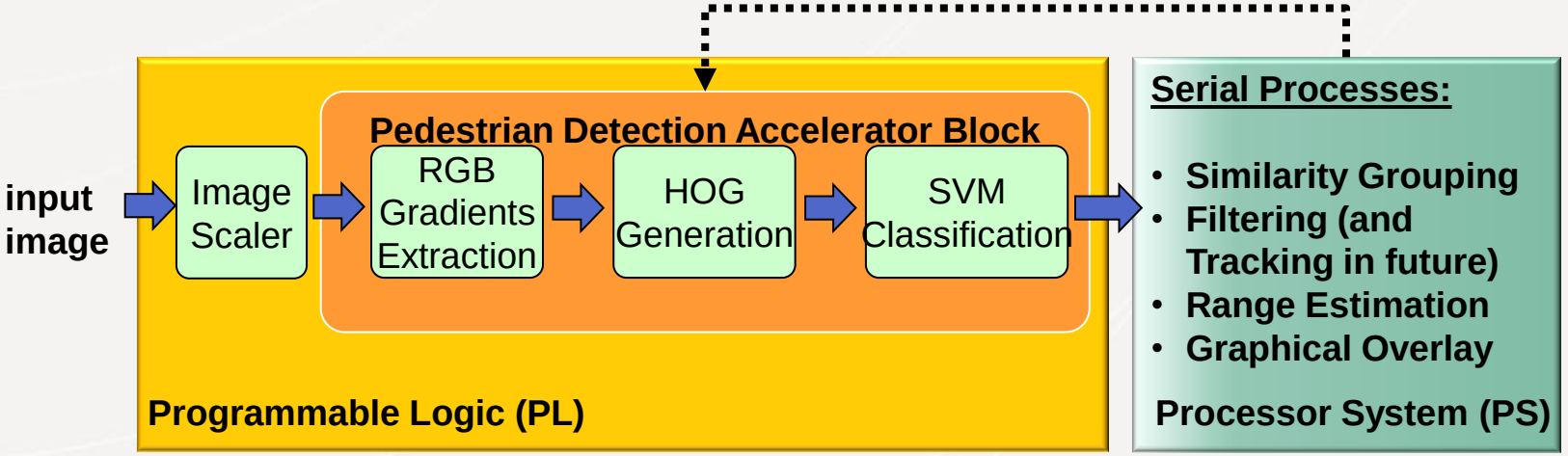
Pedestrian Detection/Classification
Acceleration Implementation Model Partitioning



Module	Slice Reg	Total LUTs	BRAM/FIFO	DSP48A1
Scaler for Pedestrian Detection Sequence	1094	1664	6	2
Pedestrian Detection HoG/SVM Core	7999	7567	37	35
Total:	9093	9231	43	37
	Slice Reg	**LUTs**	**BRAM/FIFO**	**DSP48A1**
Required	9093	9231	43	37
XAZ7020	106400	53200	140	200
% Utilization	9%	17%	31%	19%

NOTES:

1. Estimate total includes the image scaler.
2. These cores have not been optimized for size.
3. BRAM utilization is inflated as it does not account for 36K BRAM packing potential.

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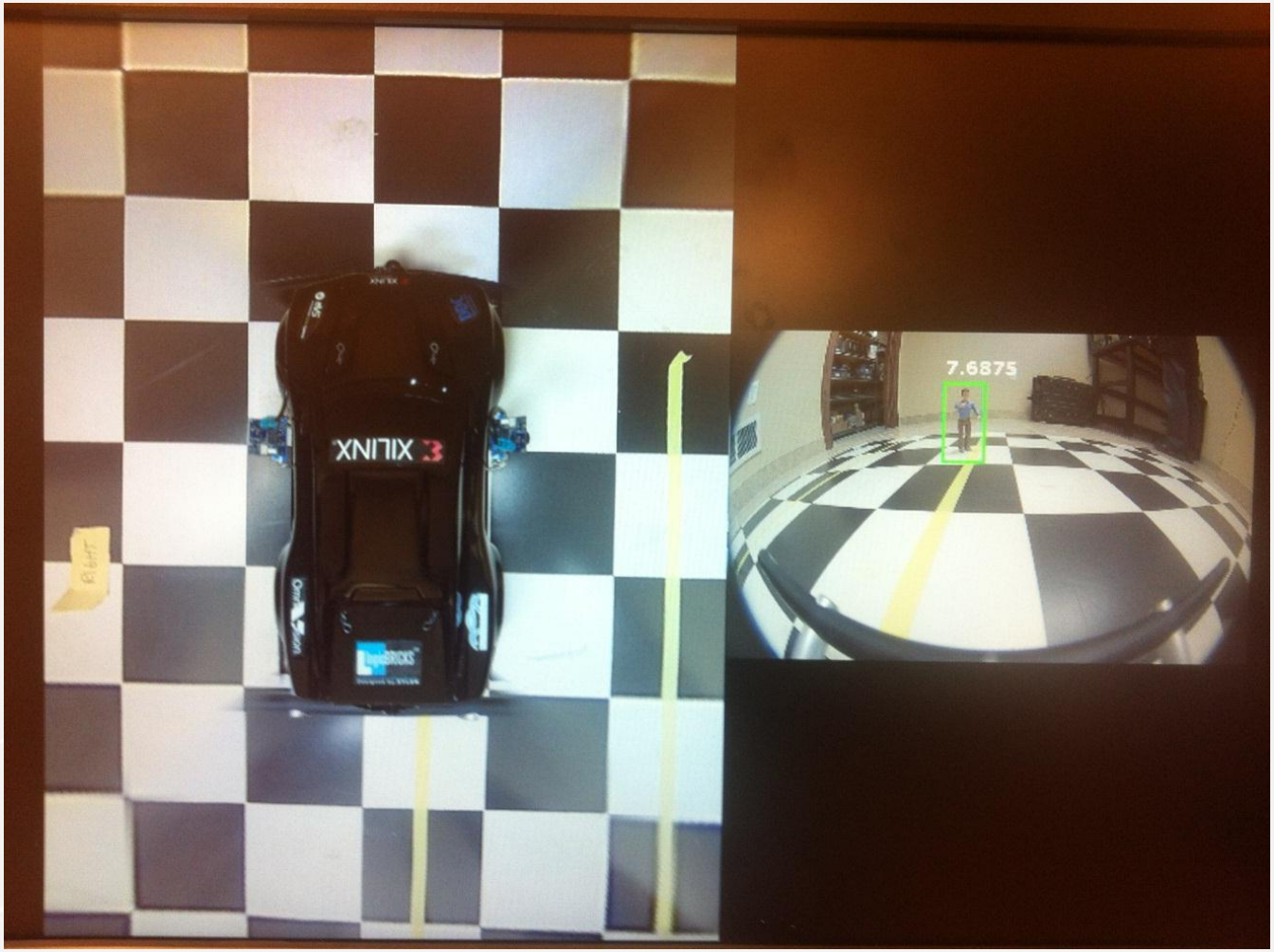
Simultaneous Multi-Feature Processing

Surround View and Pedestrian Detection



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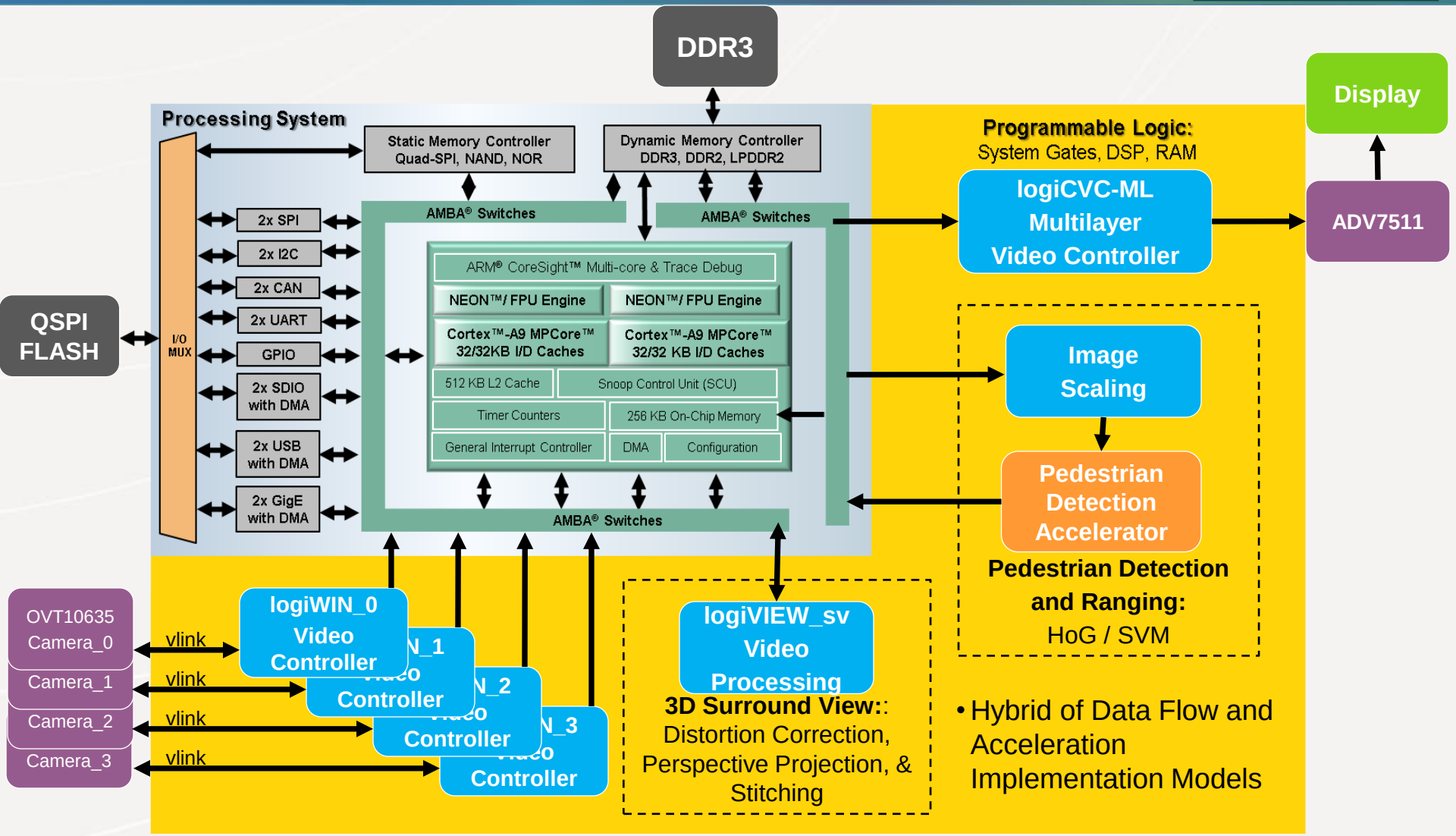
Low Speed Feature Configuration

3D Surround View, Pedestrian Detection (and Ranging)



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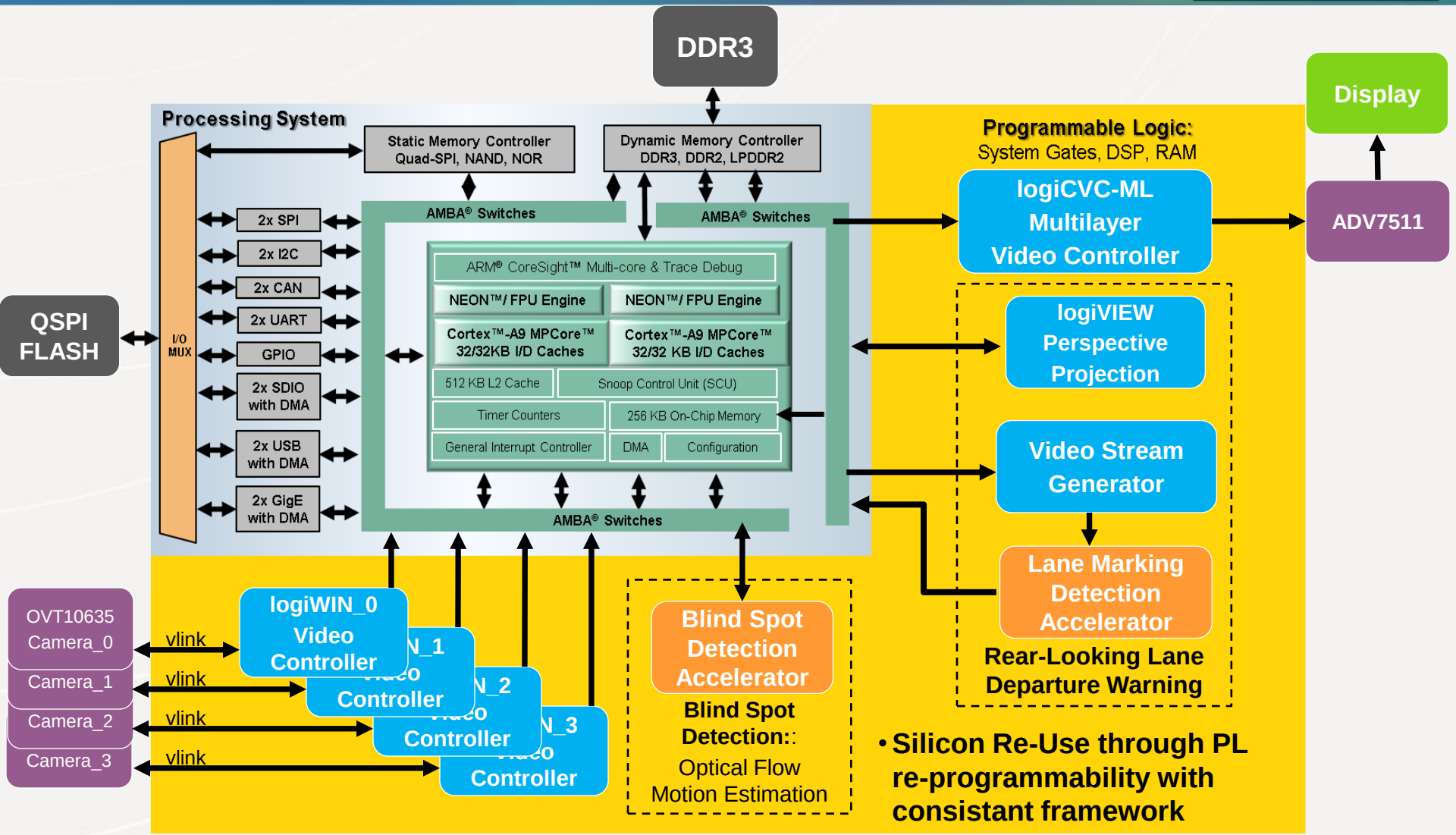
High Speed Feature Configuration
Blind Spot Detection, Rear-Looking Lane Departure Warning



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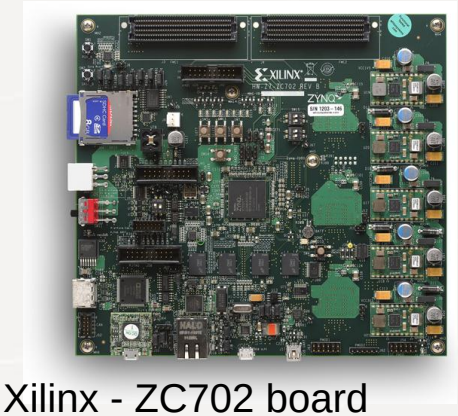
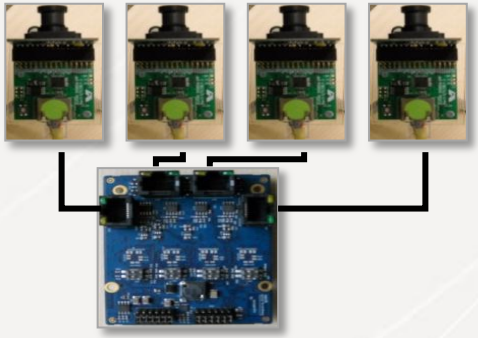
Result: Multi-Camera/Multi-Feature Platform
LogiADAK

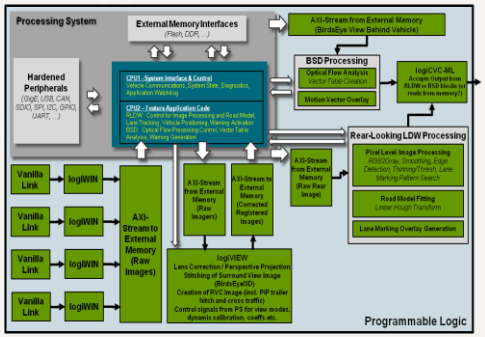
Automotive Driver Assistance Kit



Xilinx - ZC702 board



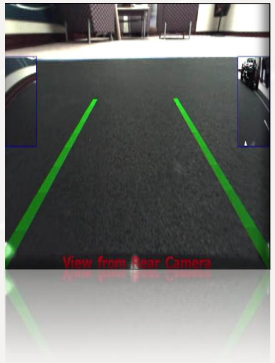
Xylon - daughter card + cameras



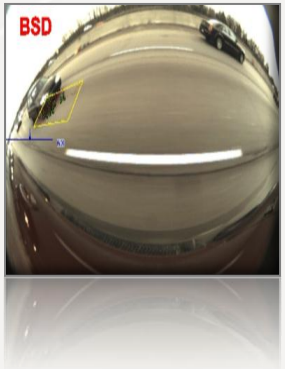
Licensable Partner IP

- 3D Surround

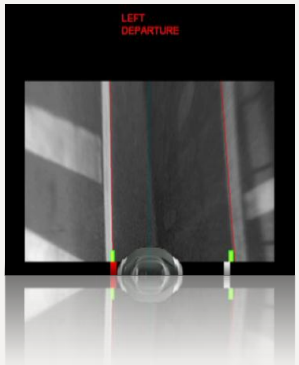
- Rear view camera with PiP



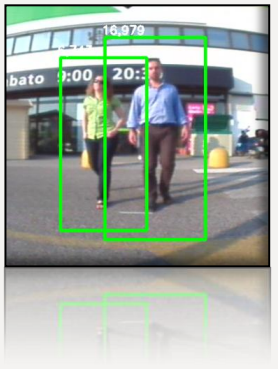
- Blind-spot with optical flow



- Rear LDW



- Pedestrian detection



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Resources for Further Investigation

- Embedded Vision Alliance Automotive Web-Page:
  http://www.embedded-vision.com/applications/automotive
- Xilinx Automotive Web-Page:
  http://www.xilinx.com/applications/automotive/index.htm
- Xylon logiADAK Web-Page:
  http://www.logicbricks.com/Products/logiADAK.aspx
- You are invited to visit the Xilinx table for a video demonstration

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