

Implementing Real-Time Hyperspectral Imaging

Kalyanramu Vemishetty

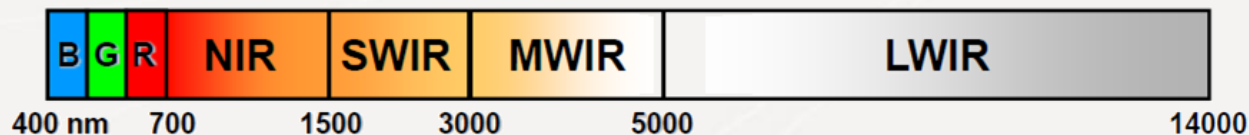
October 2, 2013

- Provider of integrated hardware and software tools to accelerate productivity, innovation, and discovery.
- \$1.14 billion in revenue in 2012
- 6,850 employees in 40+ countries
- No industry > 15% of revenue
- More than 35,000 companies served annually
- Over 16 years of vision and motion experience

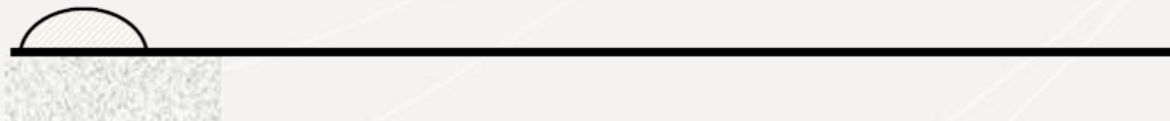


- ❑ Hyperspectral imaging and applications
- ❑ Challenges encountered with real-time implementation
- ❑ Techniques used to solve challenges
- ❑ Key lessons learned

What is Hyperspectral Imaging?



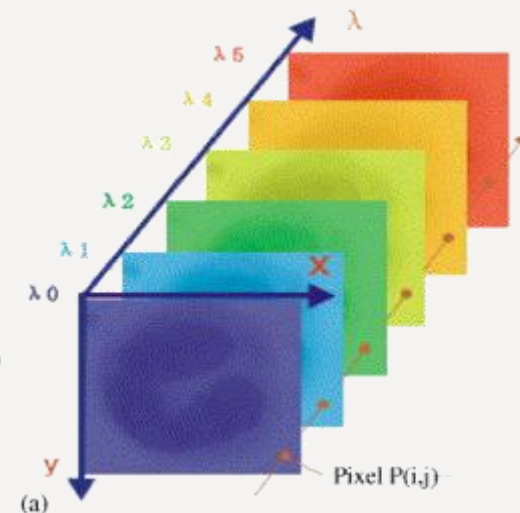
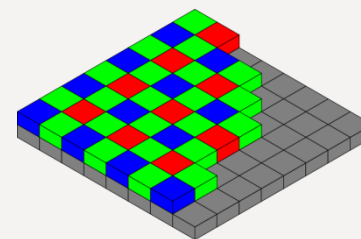
LOW **Panchromatic**: one very wide band



MED **Multispectral**: several to tens of bands



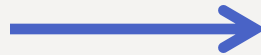
HIGH **Hyperspectral**: hundreds of narrow bands

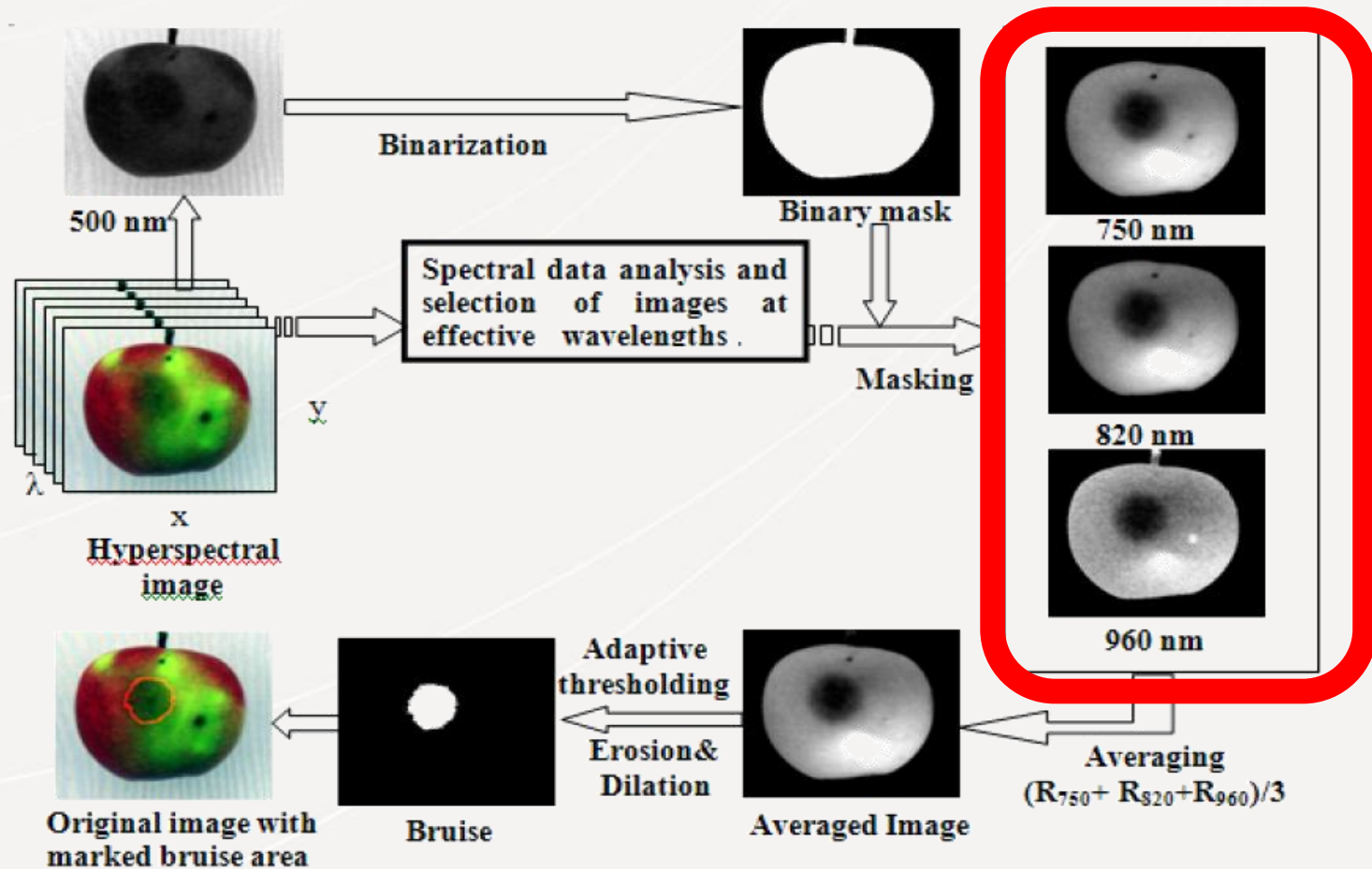


- The impact bruise may not be visible immediately when the impact applies.
 - The symptom appears after a certain period of time.
- Early detection of such an impact bruise is needed in order to improve the product quality.

Image at 750nm
(Near Infrared Spectrum)

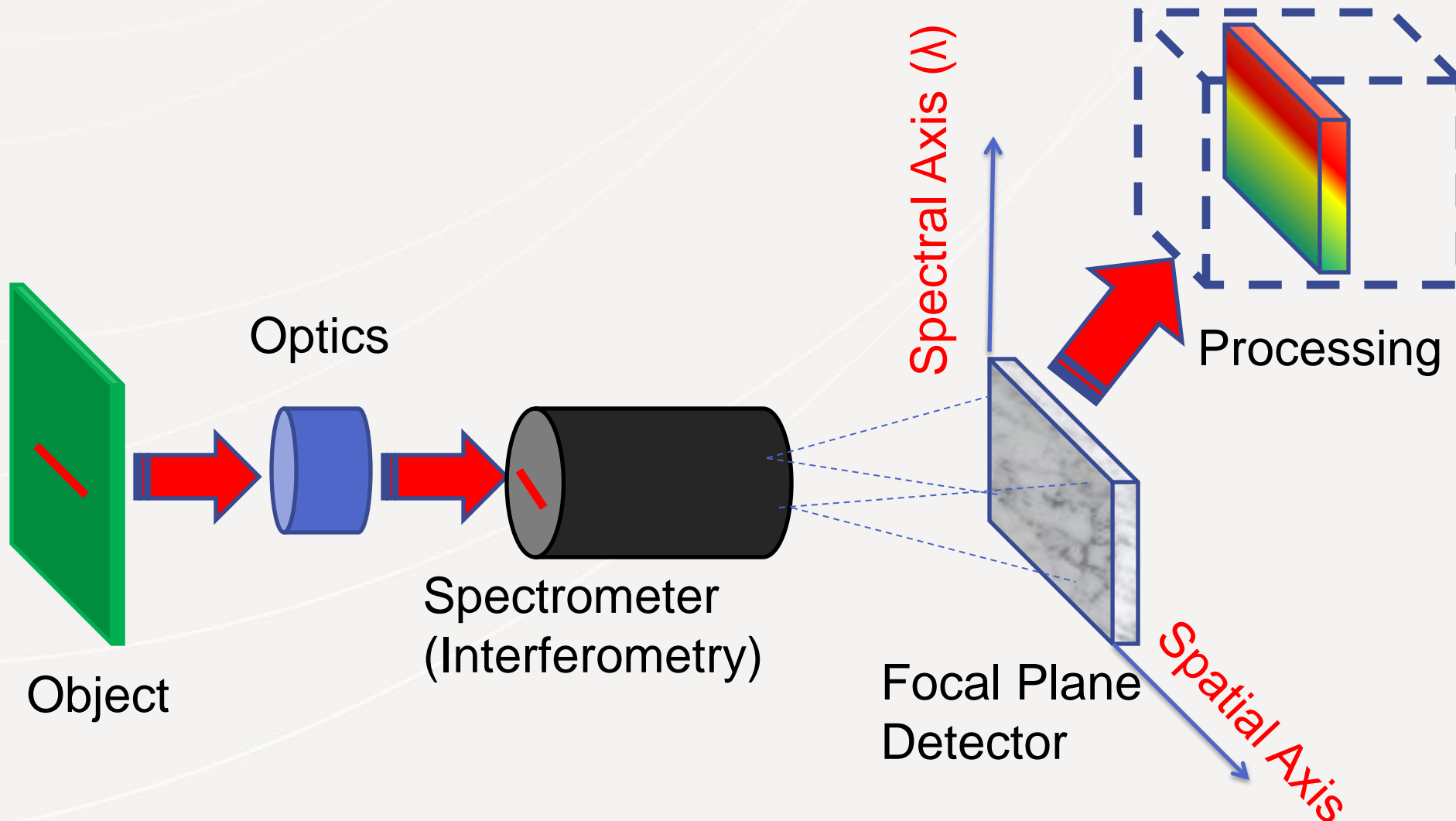
RGB Image
(Visible Spectrum)



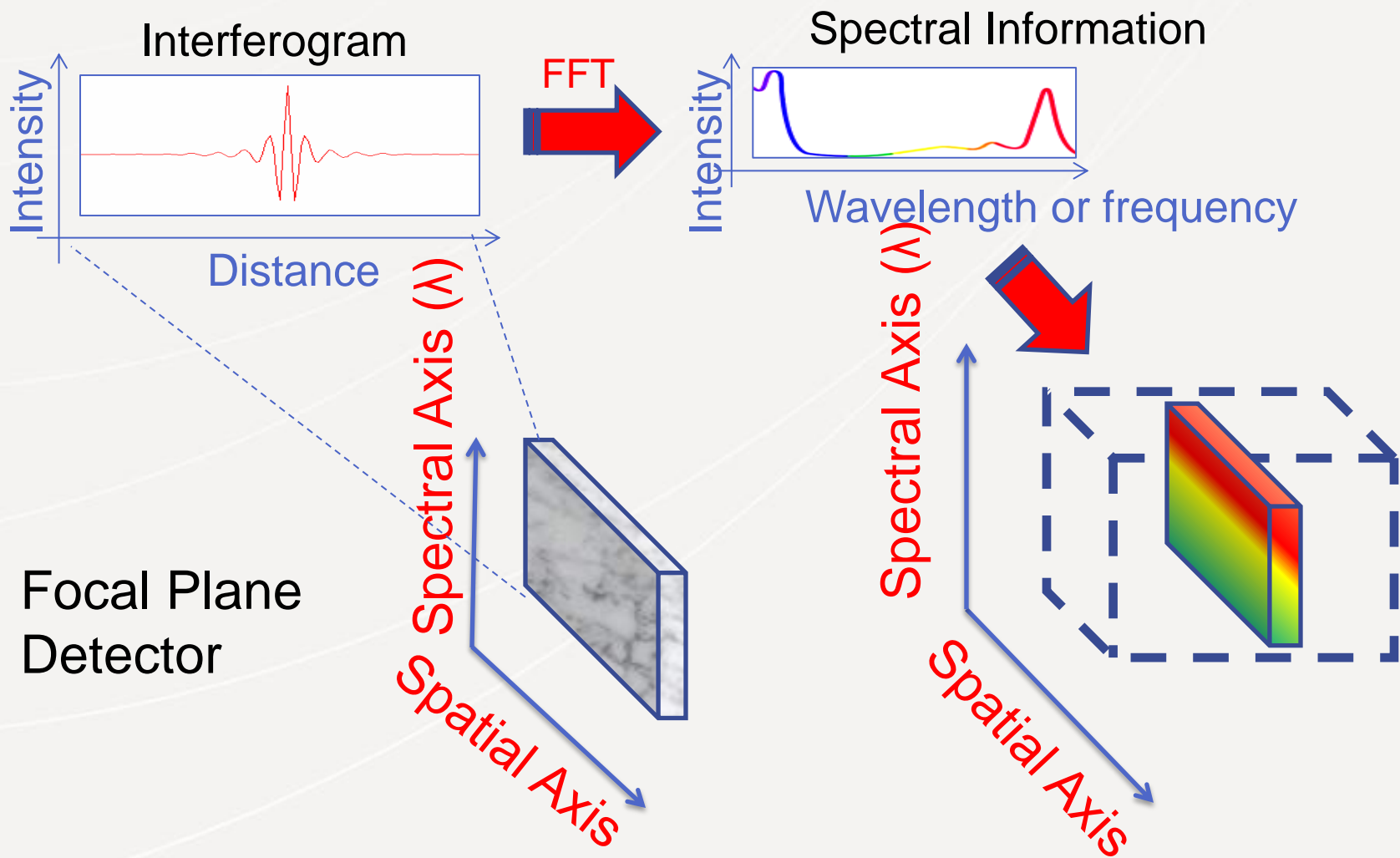


Source: Hyperspectral Images Application

Internals of Hyperspectral Imaging



Internals of Hyperspectral Imaging



Hyperspectral Imaging on Manufacturing Line

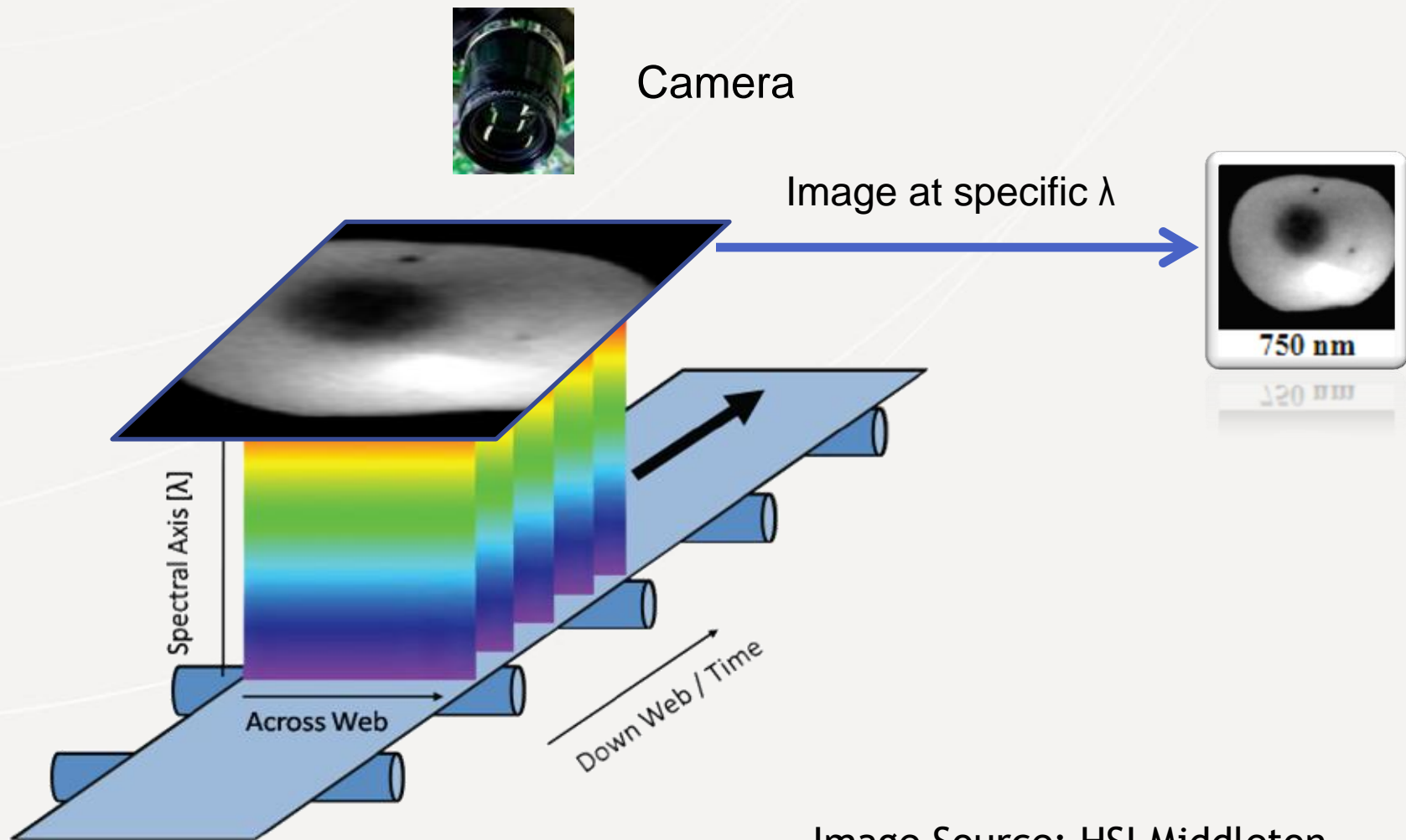


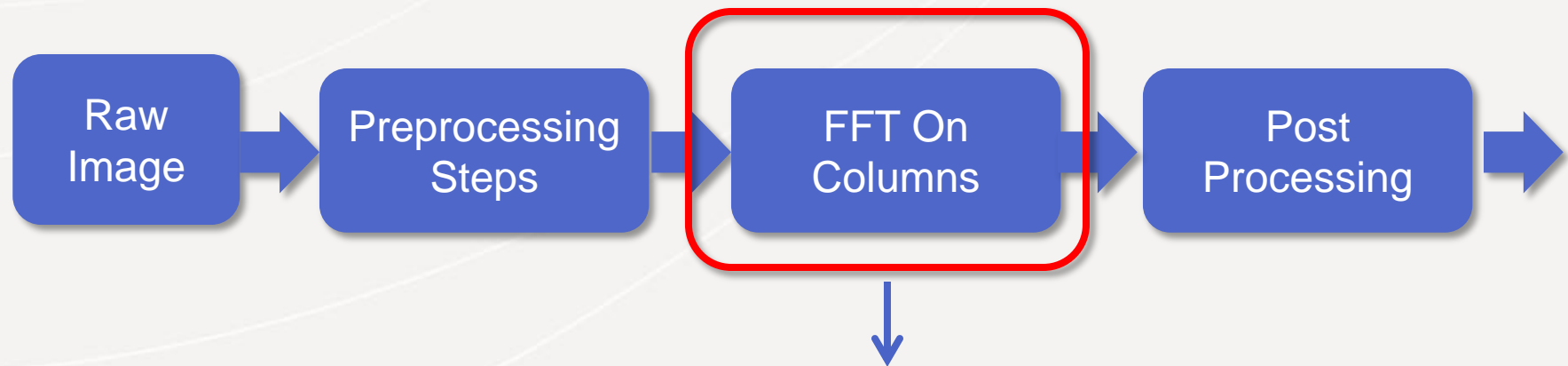
Image Source: HSI Middleton

Hyperspectral Image Processing



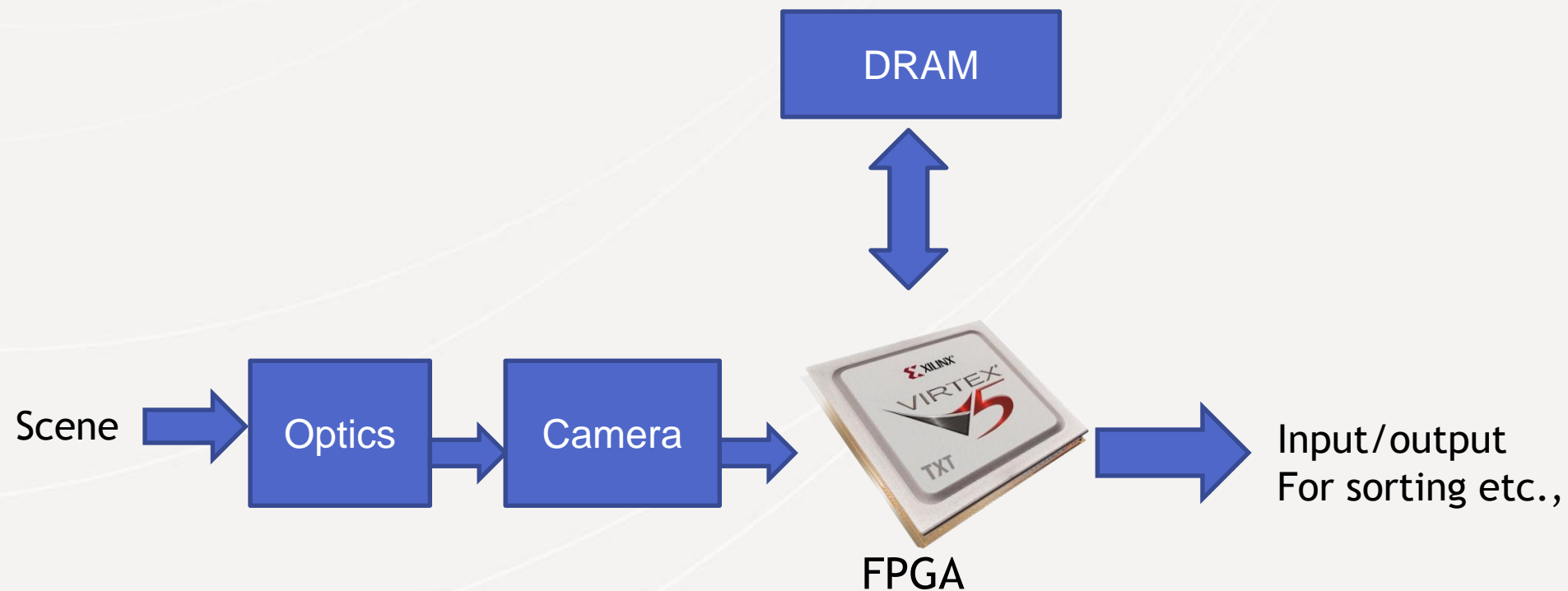
System Requirements

Image Size = 1,000x800 Pixels (Each Pixel = 14-bit)
Frame Rate = 300 Frames/sec
Data Throughput ~ 600 MB/s



Due to Fourier Transform-based Spectrometer

Application System Diagram



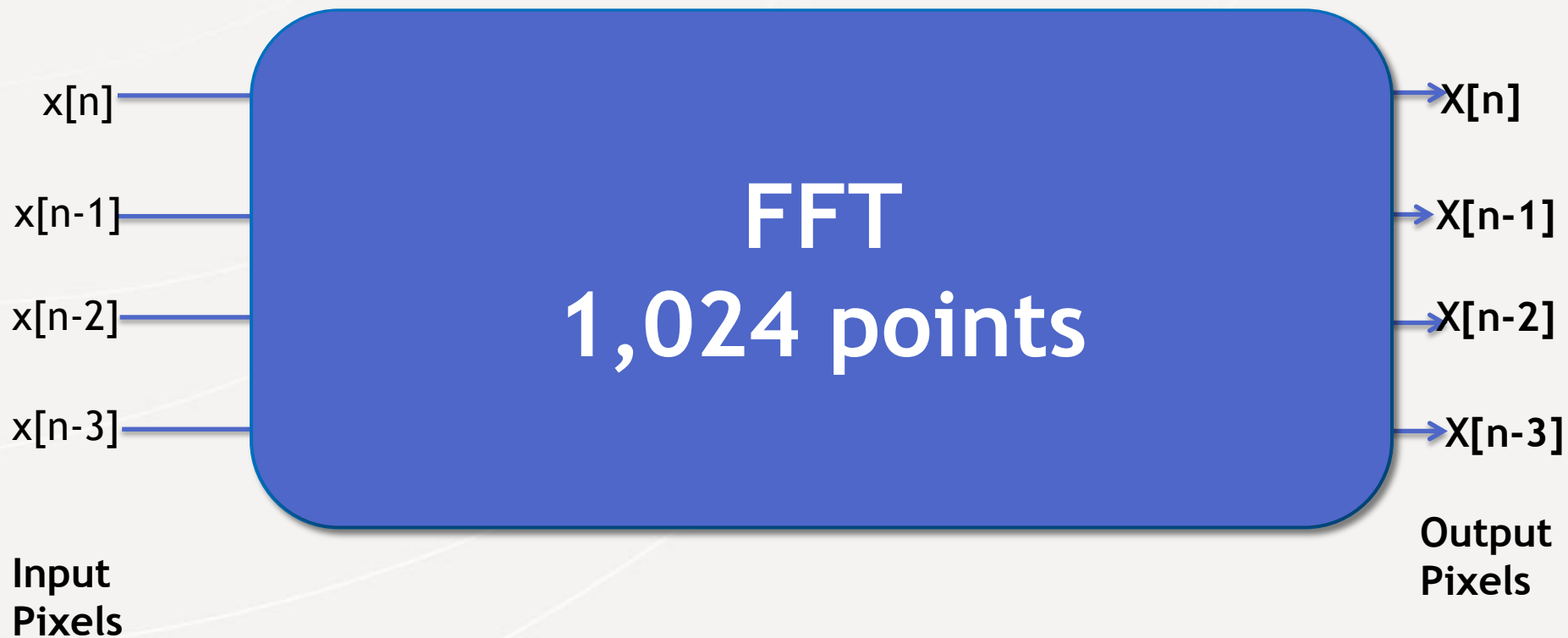
Single Pixel
@300 MHz



Camera configuration used: 4 pixels at 75 MHz from camera

4 Pixels
@75 MHz

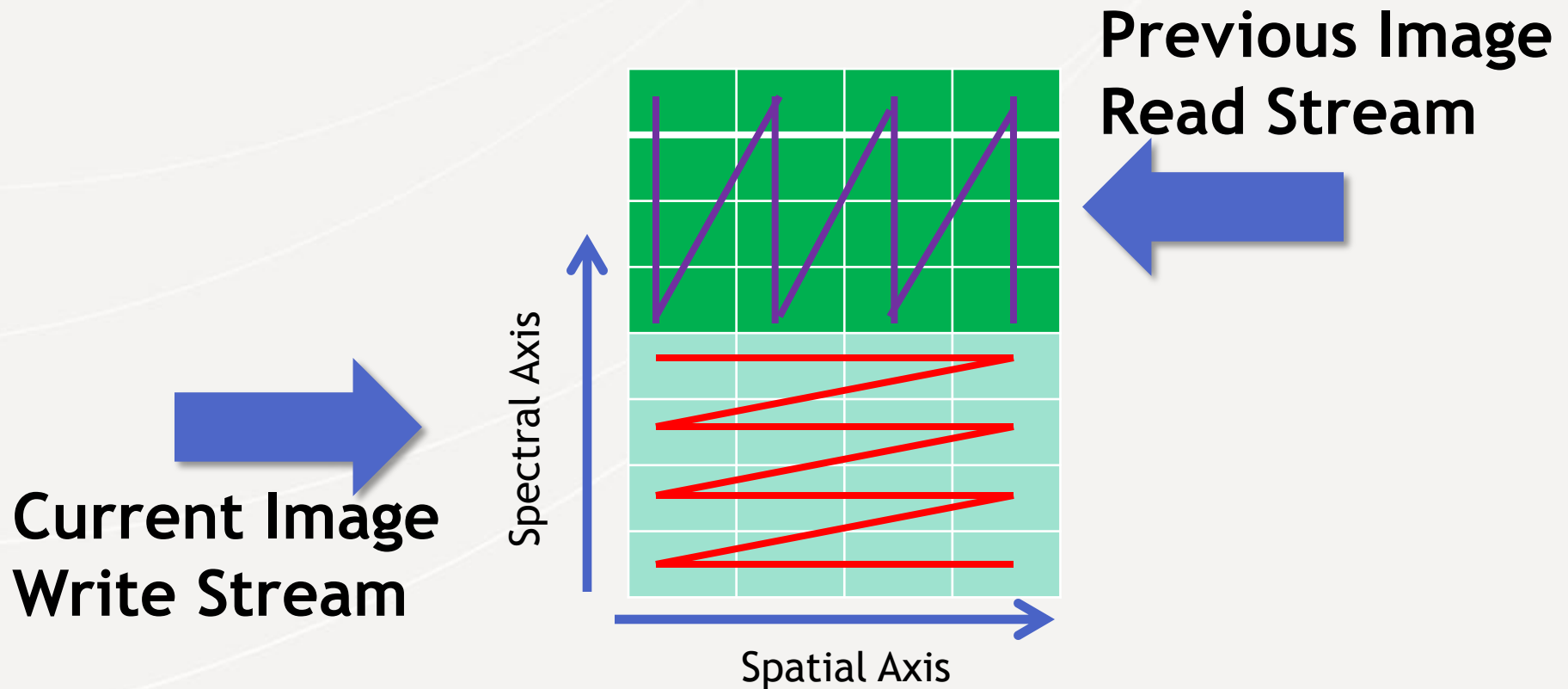




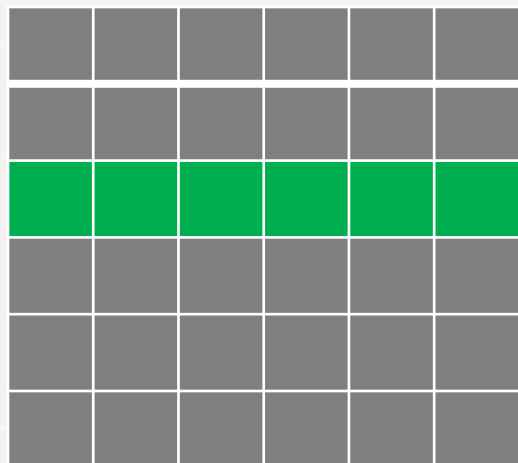
FPGA Parallel Processing for High Speeds

Streaming Image (Matrix) into Memory

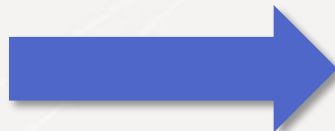
- Double buffering
- Processing in parallel with image acquisition
- DRAM read and write share time slots



Accessing elements of Column from External DRAM



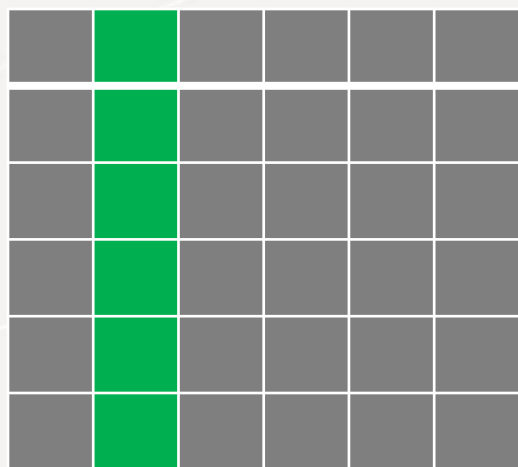
1.6 GB/s



Accesses pixels along rows sequentially



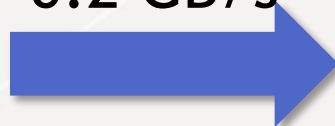
FPGA --- DRAM (from camera)



Spectral Axis

A blue arrow pointing upwards, labeled 'Spectral Axis'.

0.2 GB/s



Accesses pixels along column sequentially



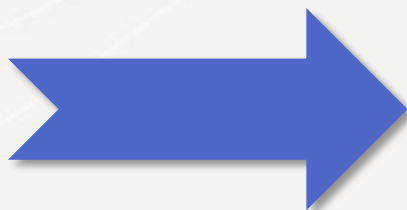
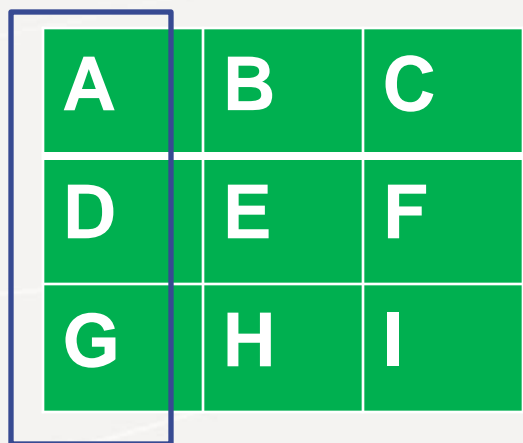
DRAM --- FPGA (for FFT)

Spatial Axis



Challenges with accessing data in Columns of Image

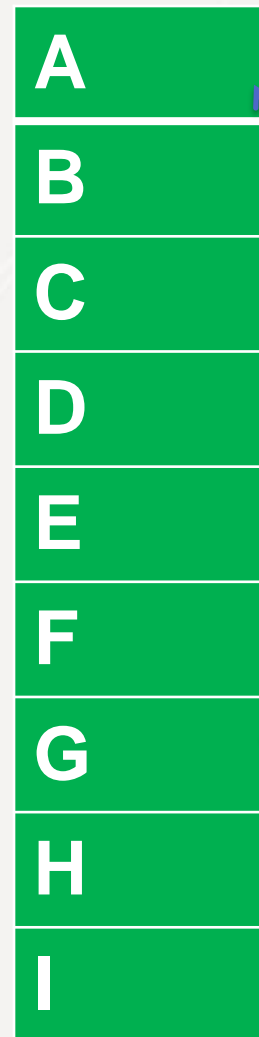
3x3 Image



0x100

0x103

0x106



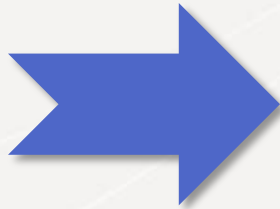
Column

Row-Wise Memory Read = 1.6 GB/s
Column-Wise Memory Read = 0.2 GB/s

Transpose

3x3 Image

A	B	C
D	E	F
G	H	I



Transposed 3x3 Image

A	D	G
B	E	H
C	F	I

0x100

0x103

0x106

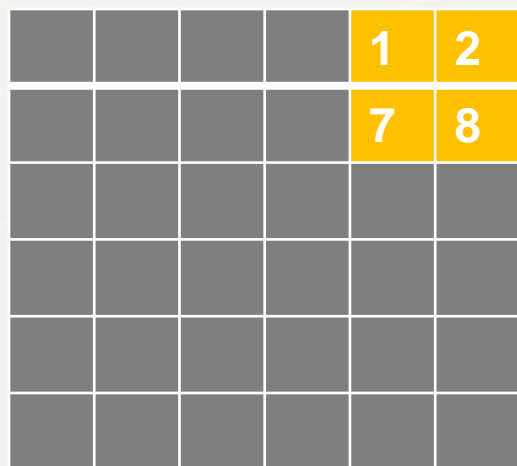
A
B
C
D
E
F
G
H
I

Accessing Points along Row Read/Write = 1.6 GB/s
Accessing Points along Column Read/Write = 0.2 GB/s

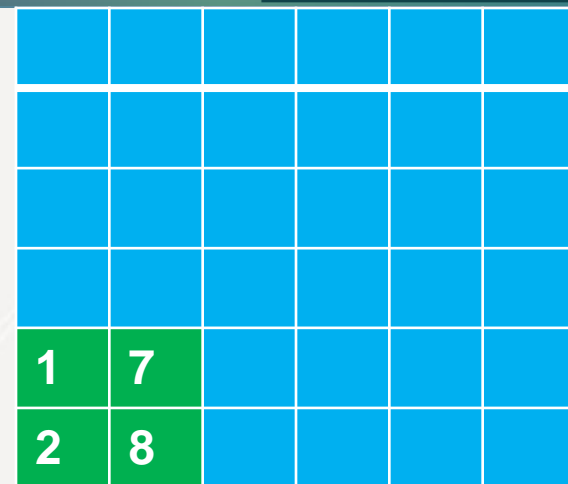
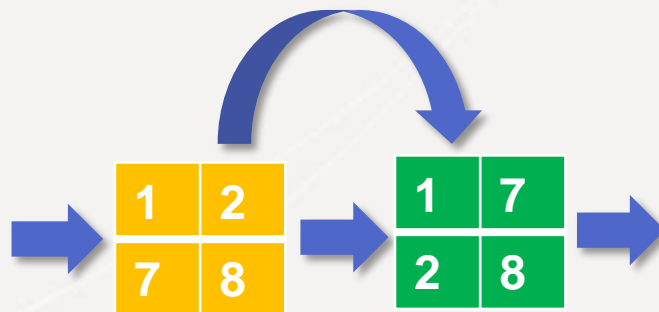
Efficient Memory Access Techniques



Matrix Transpose Tiled Approach



Raw Image



Transposed Image

Column Read	Tile Size (Pixels)	Benchmark (MB/s)
Straight Forward	Column	115
Tiled	16x16	179
Tiled	64x64	408
Tiled	128x128	532
Tiled	256x256	604

*Benchmarks are done with write time share of 50%

Camera Data Stream

A1	A2	A3	A4	A5	A6
B1	B2	B3	B4	B5	B6
C1	C2	C3	C4	C5	C6



Tile Width

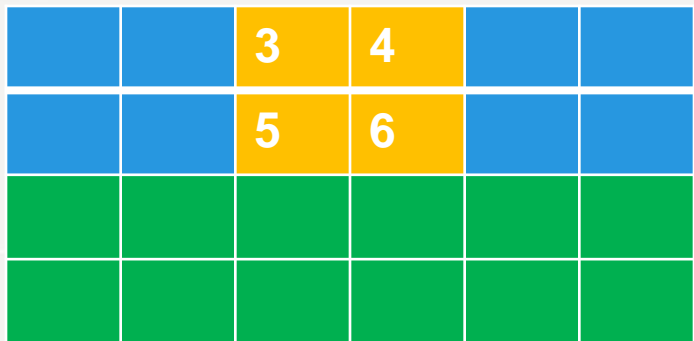


A1	B1	C1	
A2	B2	C2	
A3	B3	C3	
A4	B4	C4	
A5	B5	C5	
A6	B6	C6	



Transposed Image from DRAM for FFT

Camera Data



Most Recent 2*N Rows
(On-Chip Memory)

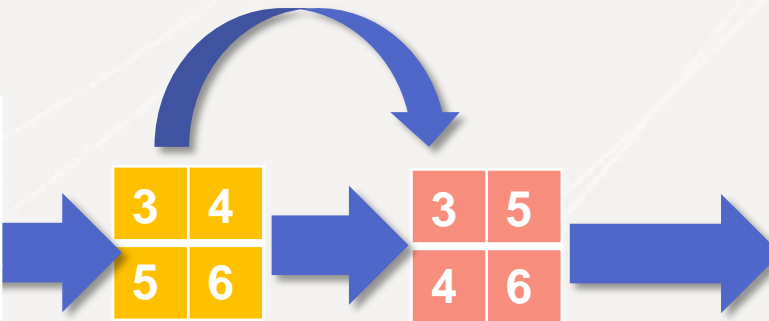
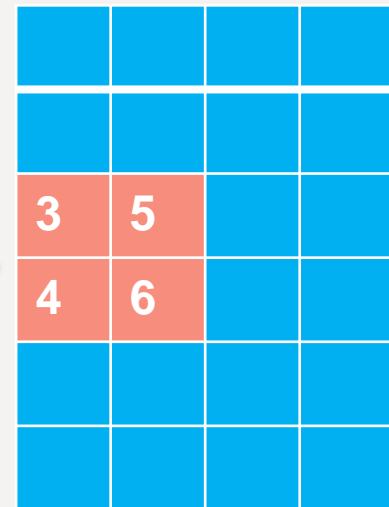


Image Storage in DRAM



DRAM Bank

Transposed Image for FFT

Camera Data

A1	A2	A3	A4	..	AN
B1	B2	B3	B4	..	BN
..
J1	J2	J3	J4	..	JN



Transposed Image (DRAM)

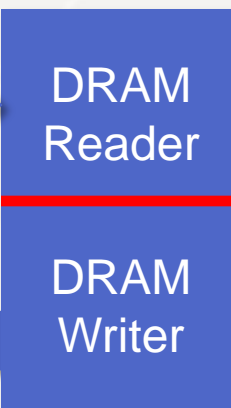
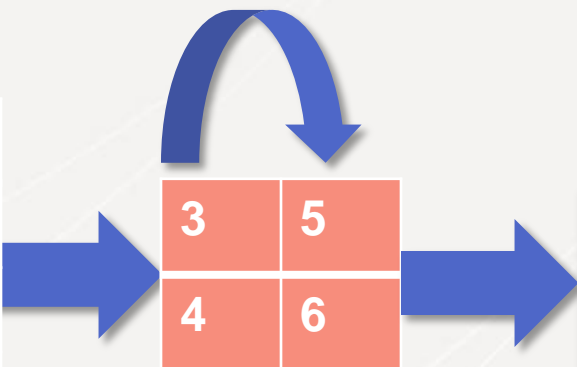
A1	B1	..	J1		
A2	B2	..	J2		
A3	B3	..	J3		
A4	B4	..	J4		
..	:		
AN	BN	..	JN		

Most Recent 2N Rows
(On-Chip Memory)

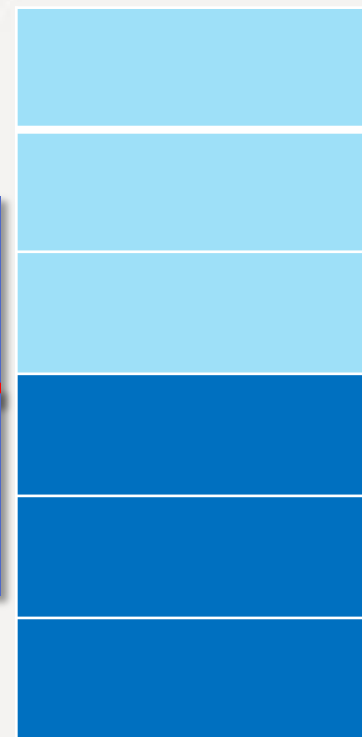
Camera Data

		3	4		
		5	6		

Most Recent 2N Rows



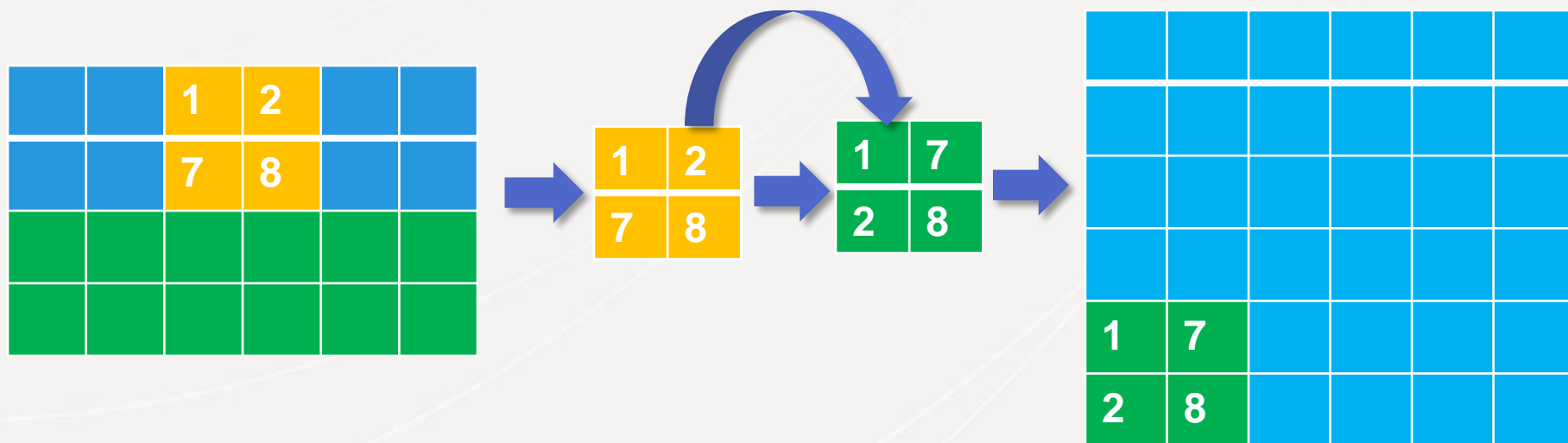
Sequential Read of
Transposed Image



DRAM Bank

DRAM writer writes tiles in columns
DRAM reader reads pixels in rows

Matrix Transpose : Resource Usage



Tiled Read	Tile Size (Pixels)	Benchmark (MB/s)	Estimated On-Chip Memory (% of Memory Used)
Straight Forward	Column	115	
Tiled	32x32	174	12.5%
Tiled	64x64	408	25%
Tiled	128x128	532	50%
Tiled	256x256	604	105%

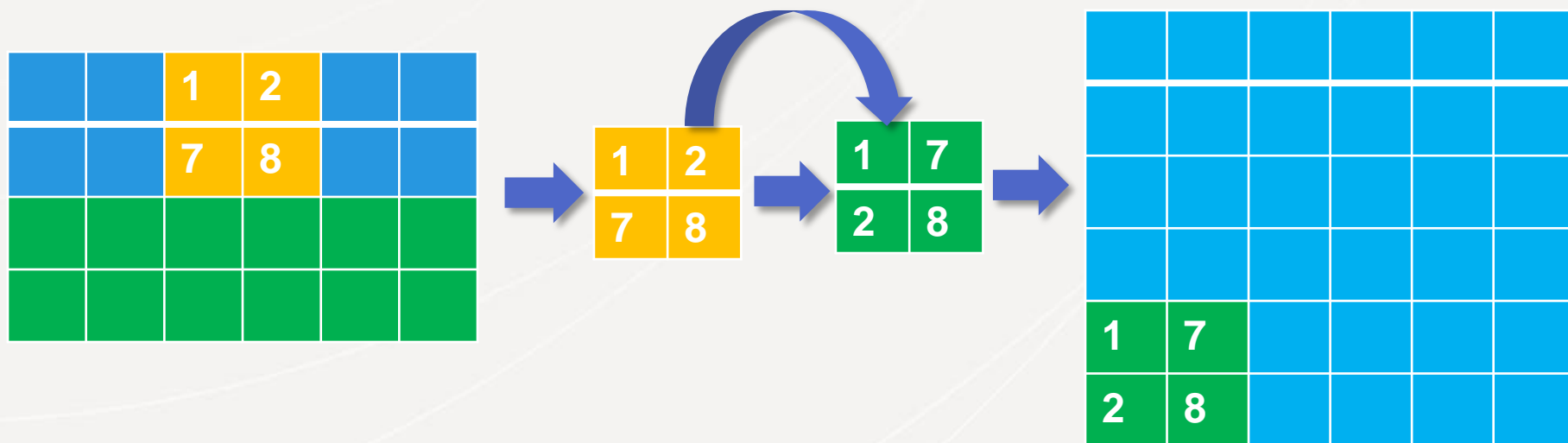
*Benchmarks are done with write time share of 50%

DRAM Time Share for Improving Throughput

- For Tile Size of 128x128:
Write Share = 50% (1us), Read Share = 50% (1us)
 DRAM Write Speed = 532 MB/s
 DRAM Read Speed = 800 MB/s
- For Tile Size of 256x256:
Write Share = 58%(1.16us) , Read Share = 42% (0.84us)
 DRAM Write Speed = 660 MB/s
 DRAM Read Speed = 640 MB/s

Tiled	256x256	604	105%
	↓		
Tiled	128x128	640	50%

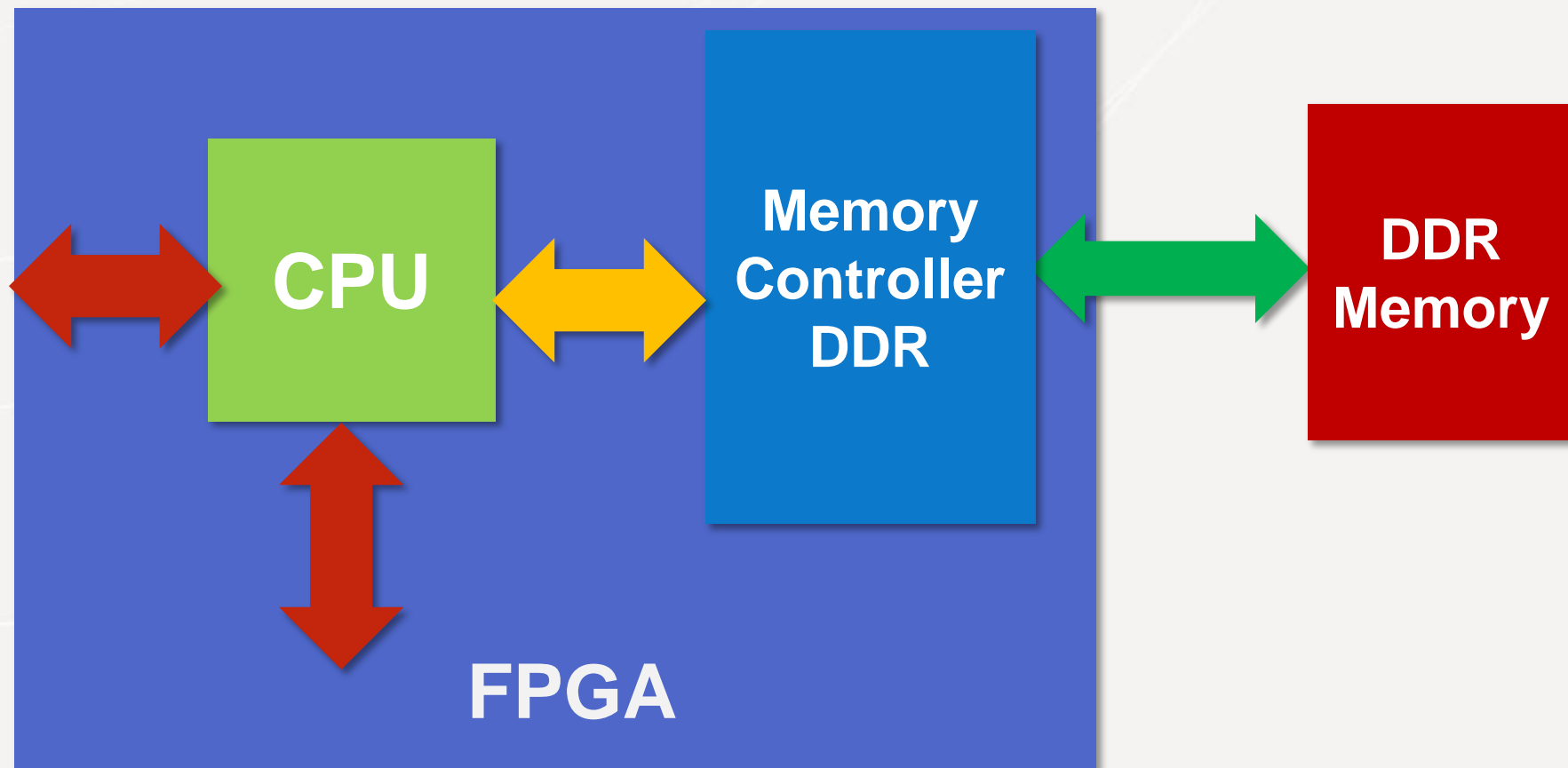
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System On Chip (FPGA+CPU on same die)



- Communication is as important as computation on embedded targets
- Understanding memory abstractions is key to image processing applications
- FPGAs with more on-chip memory are great for image processing applications

Resources for Further Investigation

- *F.Brachet, C.Buil*, “Conception and Development of Static Fourier Transform Spectrometer Breadboard”
- *Laurent Rousset-Rouviere, Christophe. Coudrain, Sophie Fabre*, “SYSIPHE, An Airborne Hyperspectral Imaging System for the VNIR-SWIR-MWIR-LWIR Region”
- *Julie Dai*, “Hyperspectral Images Applications”

NI Vision & FPGA Products

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- www.ni.com/flexrio

Embedded Vision Alliance

- www.embedded-vision.com