Abstract

Addressing System Design Challenges in Embedded Vision

Embedded vision applications need to move video data from the image sensor to processing and storage elements. When dealing with higher video resolutions and/or frame rates, this presents design challenges that need to be thought out early in the architecture phase. This class describes the challenges and some of the solutions that exist today.

Addressing System Design Challenges in Embedded Vision

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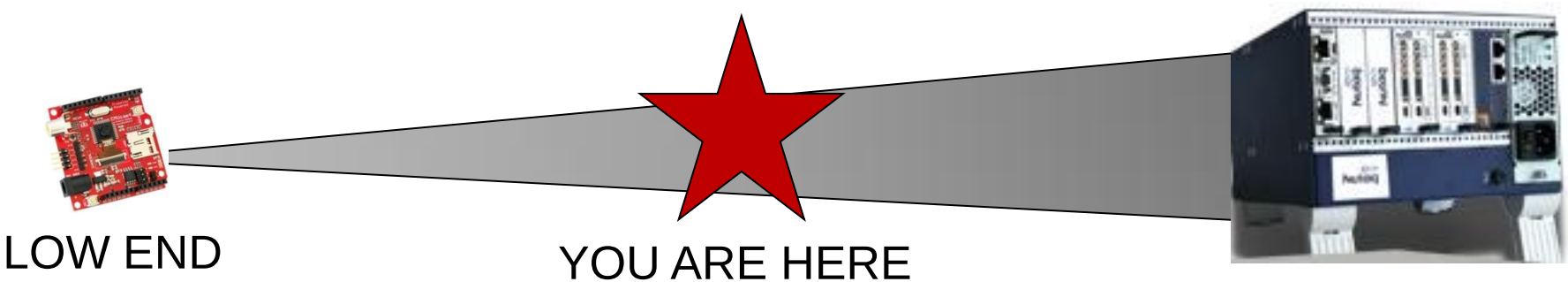
AVNET®

Introduction

- Large landscape of embedded vision solutions
  - Low-end : lower performance, very low cost
  - High-end : higher performance, very high cost/power



- Challenge zone
  - Moderate to high perf., moderate to low cost/power
- This session will cover
  - Challenges involved in moving data around in an embedded vision system

Case Study – VITA image sensor

- VITA family overview
  - **Global shutter** and rolling shutter
  - High pixel rate image sensors

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Image Sensor	Active Area	Frame Rate	Throughput
VITA-1300	1280 x 1024	150 fps	2.5 Gbps
VITA-2000	1920 x 1200 640 x 480 256 x 256	92 fps 555 fps 1730 fps	2.5 Gbps
VITA-5000	2592 x 2048	75 fps	5 Gbps
VITA-25K	5120 x 5120	53 fps	20 Gbps

- Video throughput = resolution * frame rate
  - VITA-2000 => 250 M pixels/sec
  - VITA-25K => 2 G pixels/sec

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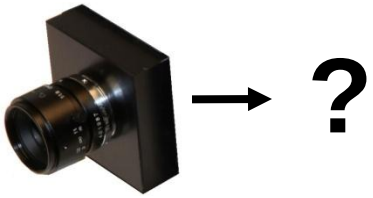
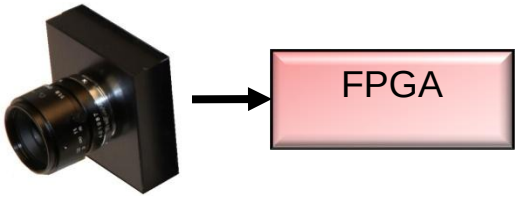
The image sensor interface

- Challenge



  - Parallel interfaces
    - Higher pin count, higher power consumption
    - Single-ended signaling : feasible up to 100 MHz per pin
    - Typically limited to 30 frames/sec for HD video
- Solution
  - Serial interfaces
    - Lower pin count, lower power consumption
    - Differential signaling : feasible up to 1 Gbps per pair
    - Scalable using multiple pairs
      - VITA-2000 => 4 data channels
      - VITA-25K => 32 data channels

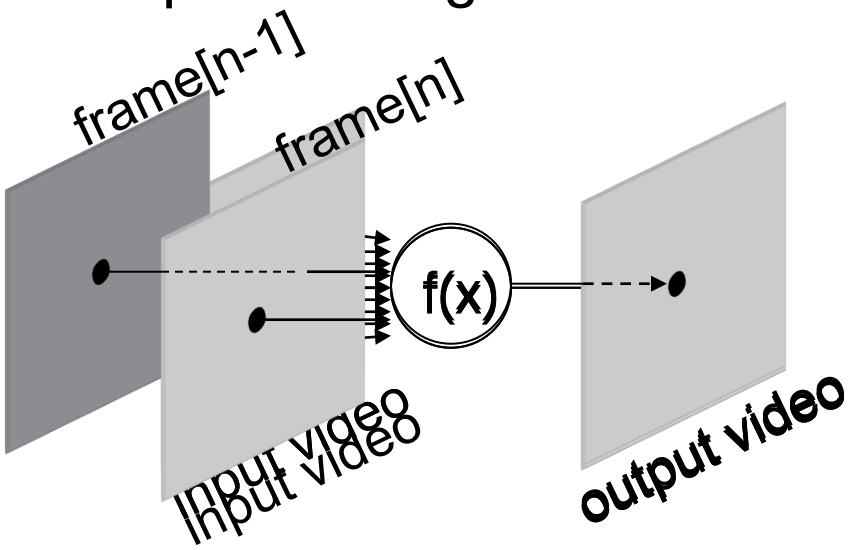
Receiving data from the image sensor



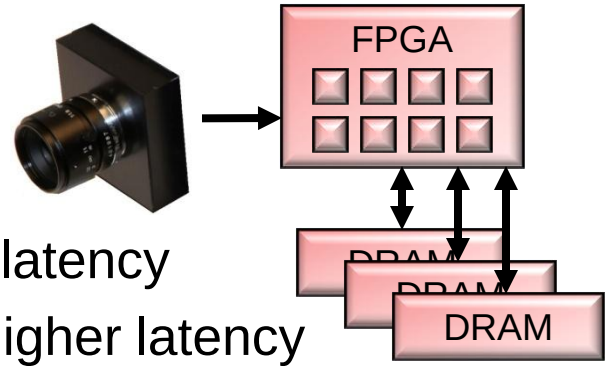
- Challenge
  - Serial interfaces
    - Can be proprietary
    - May not be available on processors/DSPs
- Solution
  - FPGA
    - Easy to implement with programmable logic
    - Inherently parallel processing nature of FPGA scales well to VITA family
      - VITA-2000 => 62 M pixels/sec * 4 data paths
      - VITA-25K => 62 M pixels/sec * 32 data paths

Moving data to/from memory

- Video storage
  - Video processing algorithms require storage
    - Pixel processing
      - No storage required
    - Spatial processing
      - Line buffers required
    - Temporal processing
      - Frame buffers required
  - Memory requirements
    - Size
      - Depends on image size, and required history
    - Bandwidth
      - Depends on image size, frame rate, and number of times frame is accessed

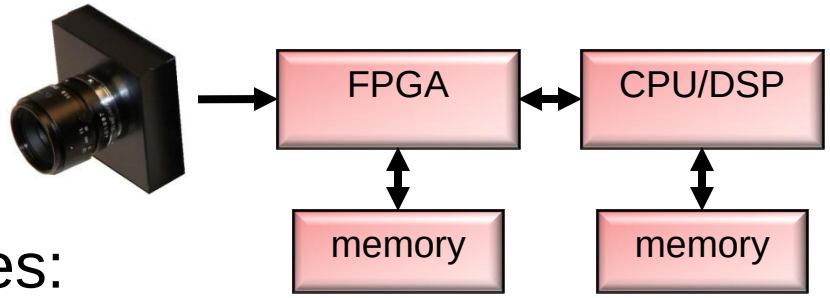


Moving data to/from memory



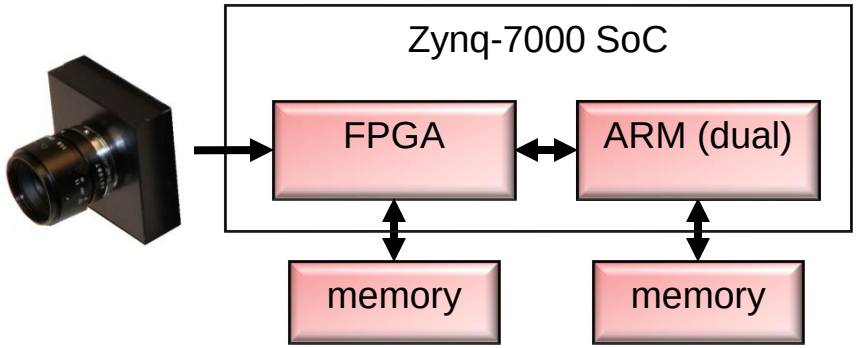
- Challenge
  - Memory typically available:
    - SRAM : on-chip, smaller size, low latency
    - DRAM : off-chip, larger capacity, higher latency
  - How to make optimal use of available memory?
- Solution
  - DRAM memory
    - Used for frame buffers
  - SRAM memory
    - Used for line buffers, parameters
    - Used as cache to improve performance of DRAM memory
  - Multiple memory interfaces

Processing the data



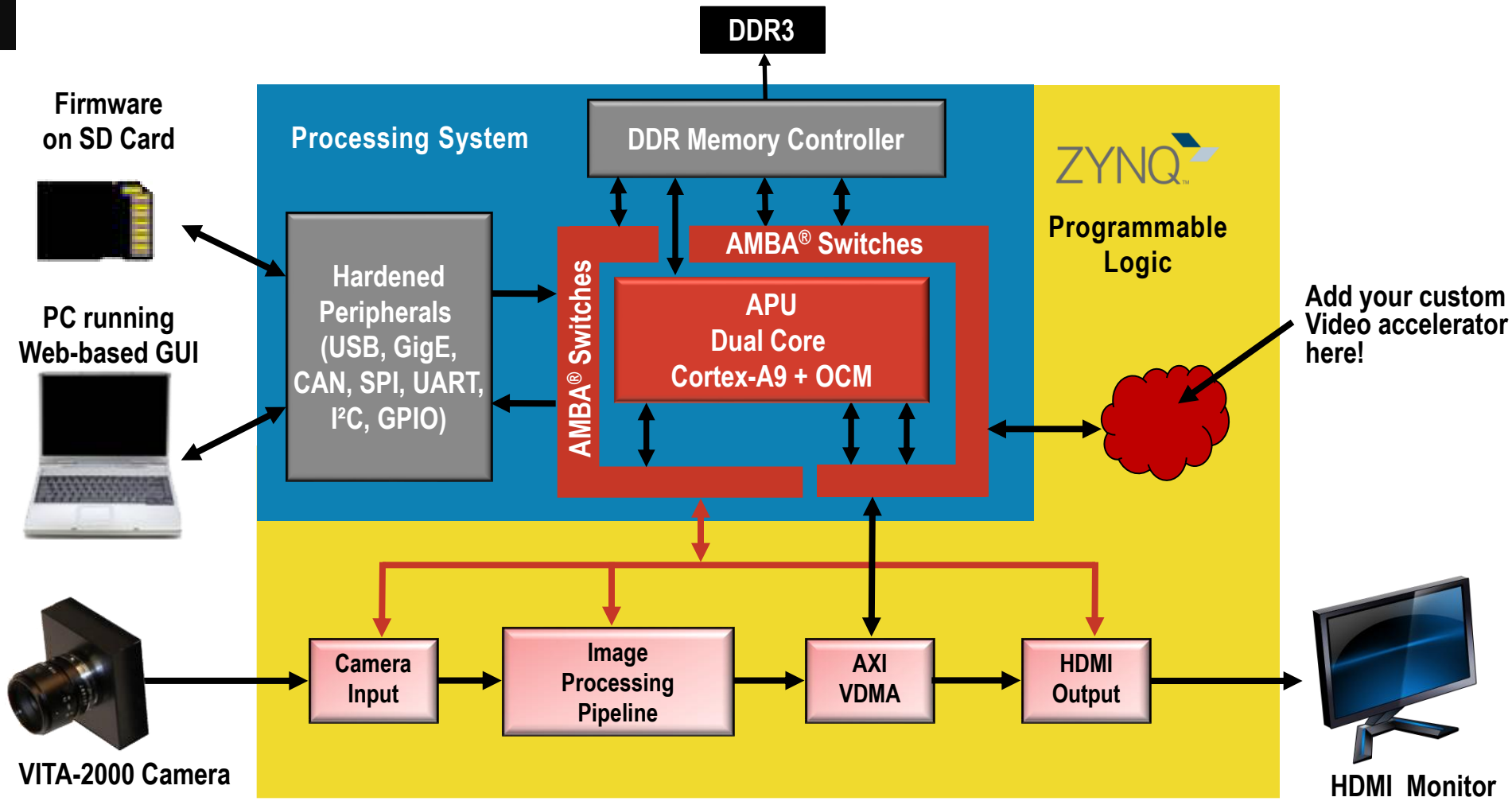
- Challenge
  - Embedded Vision requires:
    - Execute compute-intensive tasks in real time at high pixel rates
    - Perform video analytics, complex decision making and network communication
    - Leverage computer vision toolboxes (OpenCV, propriety algorithms, legacy code)
- Solution
  - FPGA executes compute intensive processing
  - Add a CPU/DSP

Moving data to/from the CPU/DSP

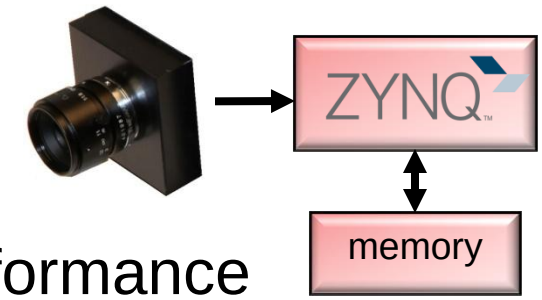


- Challenge
  - 2 chip solution
    - Simple if FPGA is only involved in pre-processing
    - Complex if FPGA is also used as a co-processor
- Solution
  - Xilinx Zynq-7000 SoC
    - Combines best of both worlds:
      - Dual core ARM Cortex-A9
      - Programmable logic

Zynq-7000 SoC based Vision Solution



Summary



- Image Sensor Interfaces
  - Serial interfaces offer higher performance
- FPGA technology offers
  - High performance video processing
  - Flexible memory solutions
  - Flexible, high performance sensor interfaces
- Highly integrated devices combine
  - FPGA technology
  - Industry standard processors